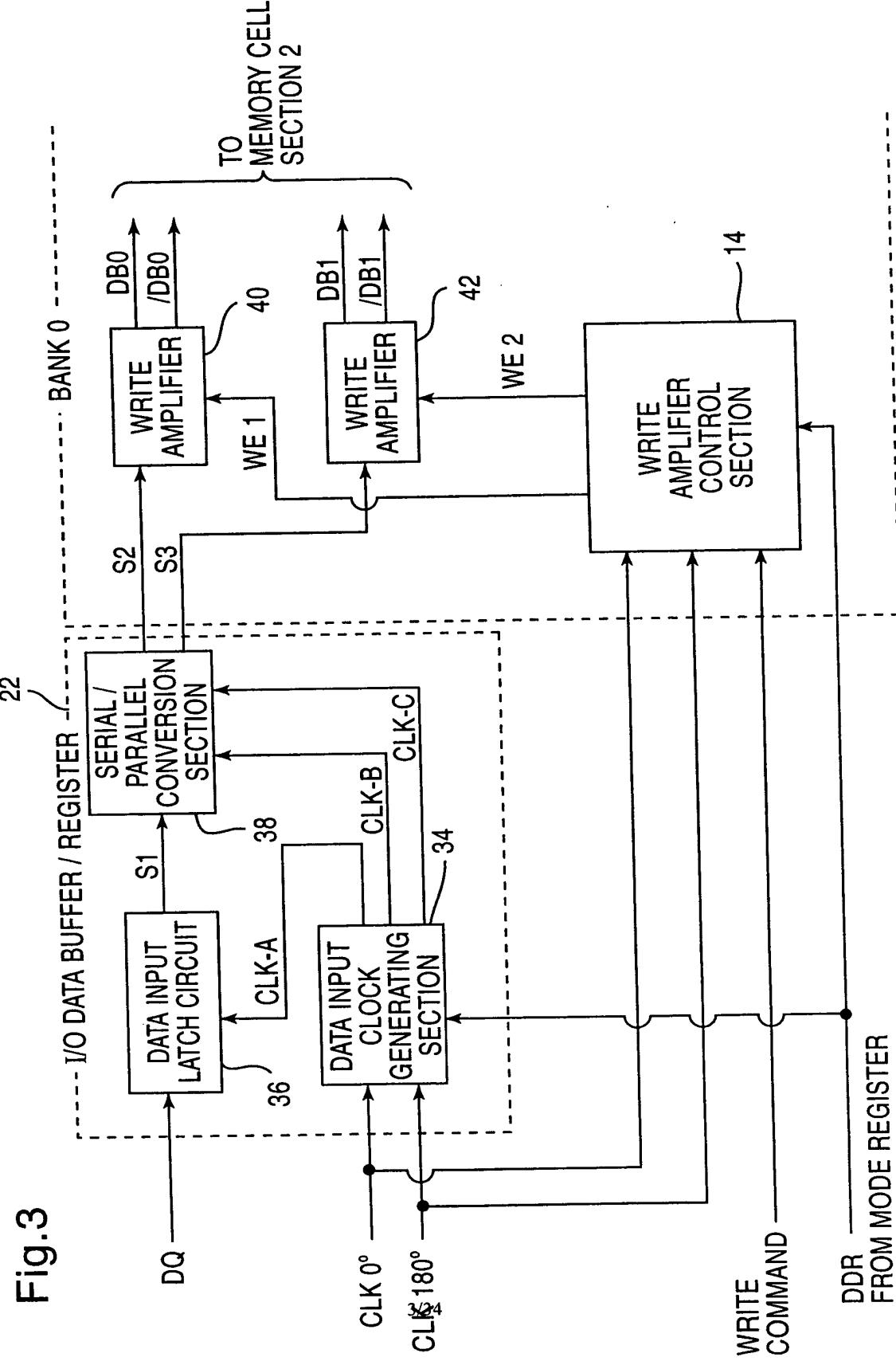


Fig.2

COMMAND FUNCTION NAME	COMMAND	CKE	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	A11	A10	A9 ~ A0
	n - 1	n							
NON-SELECTION OF DEVICE	DESL	H	X	H	X	X	X	X	X
NO OPERATION	NOP	H	X	L	H	H	X	X	X
READ	READ	H	X	L	H	L	H	V	V
READ / AUTO PRECHARGE	READA	H	X	L	H	L	H	V	V
WRITE	WRIT	H	X	L	H	L	V	L	V
	WRITA	H	X	L	H	L	V	H	V
WRITE / AUTO PRECHARGE									
BANK ACTIVE (RAS)	ACTV	H	X	L	L	H	H	V	V
SINGLE BANK PRECHARGE	PRE	H	X	L	L	H	L	V	X
ALL BANK PRECHARGE	PALL	H	X	L	L	H	L	X	X
MODE REGISTER SET	MRS	H	X	L	L	L	L	V	V



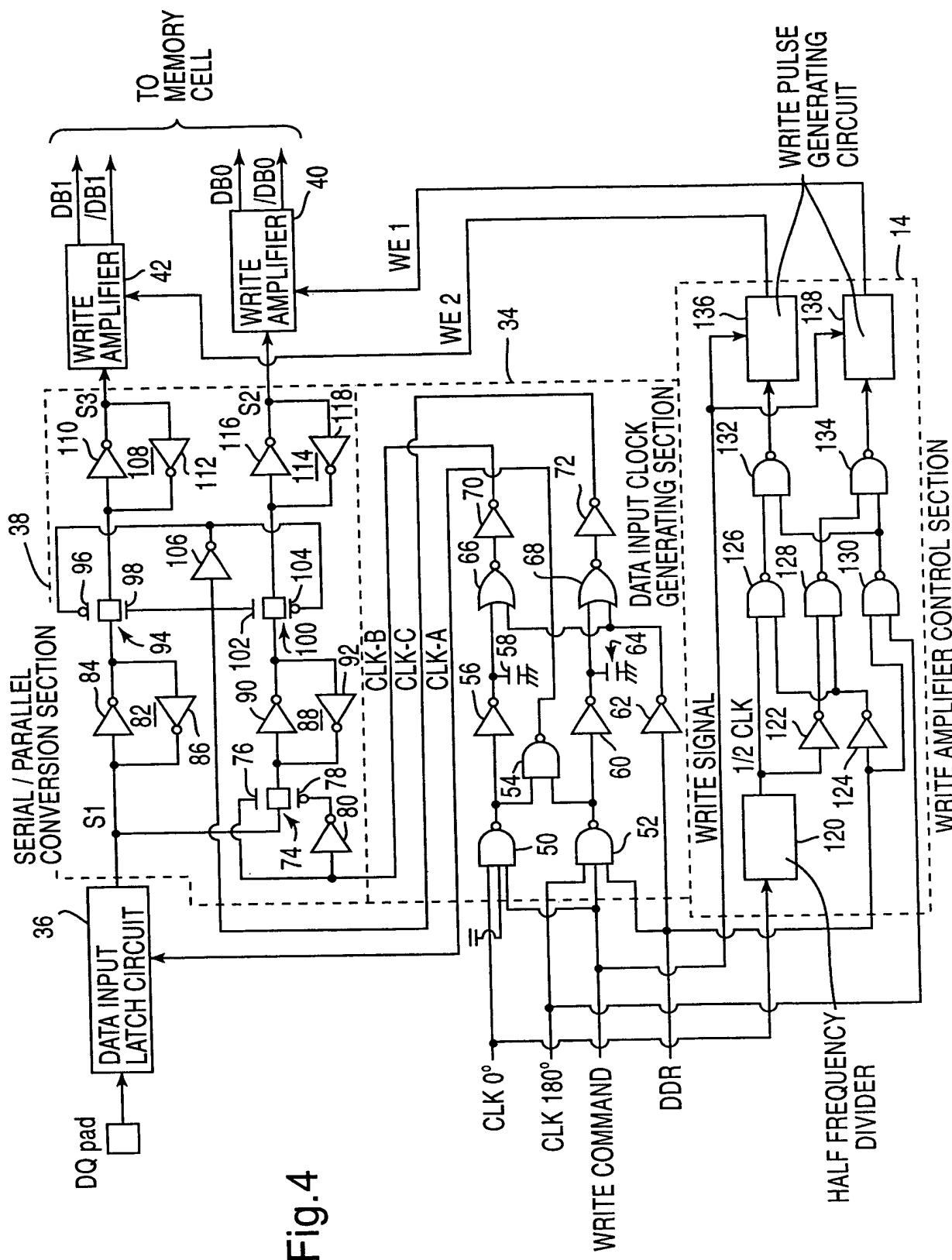


Fig.5

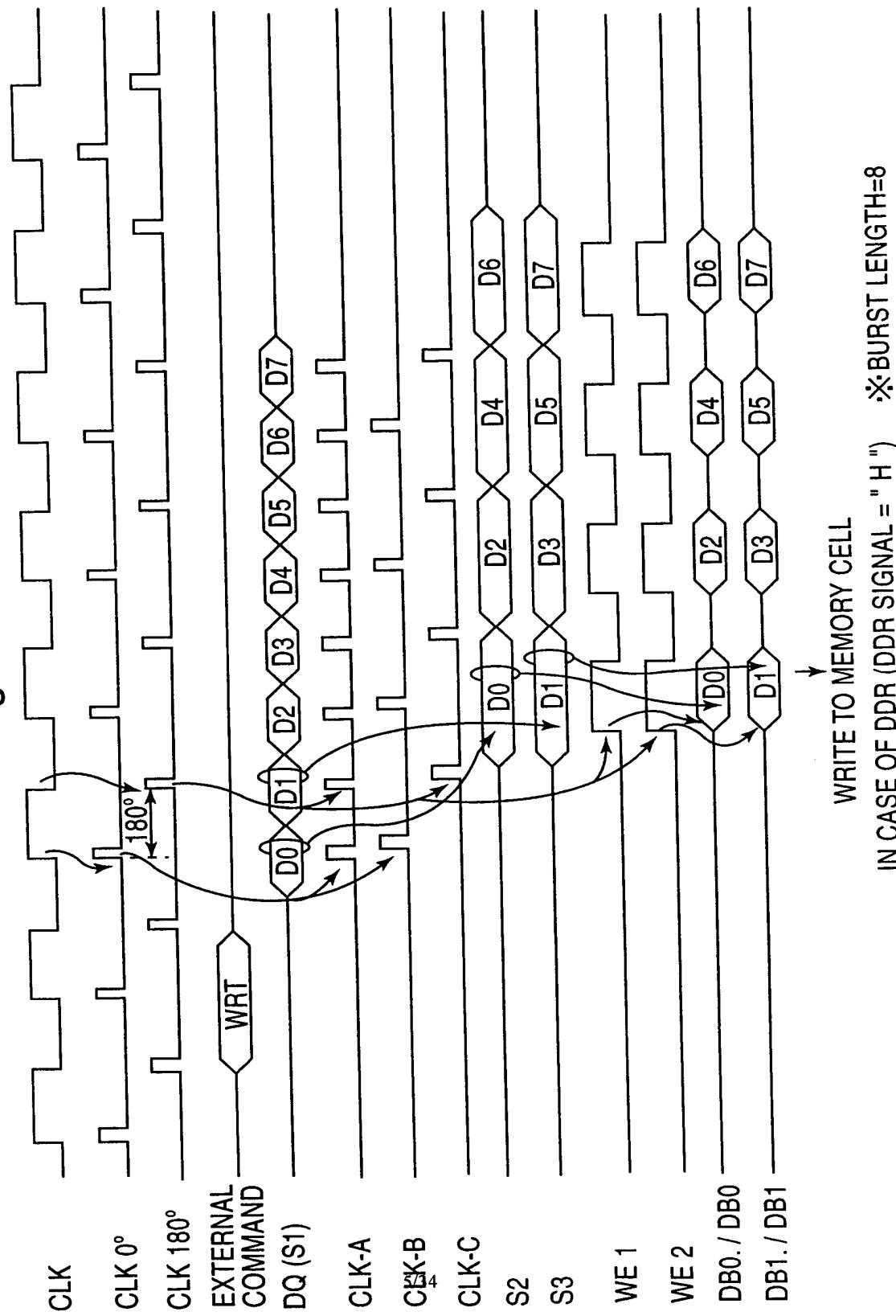
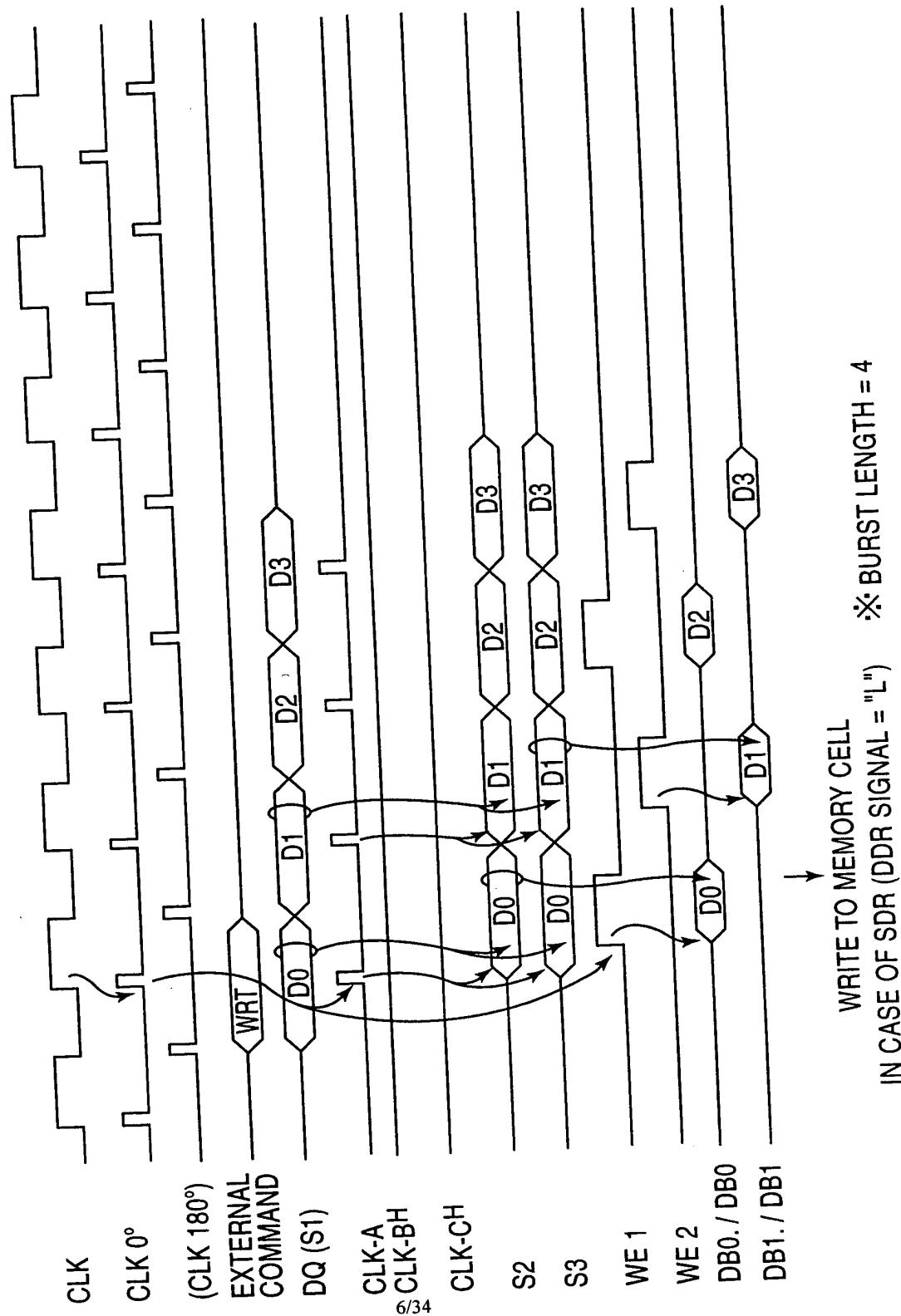
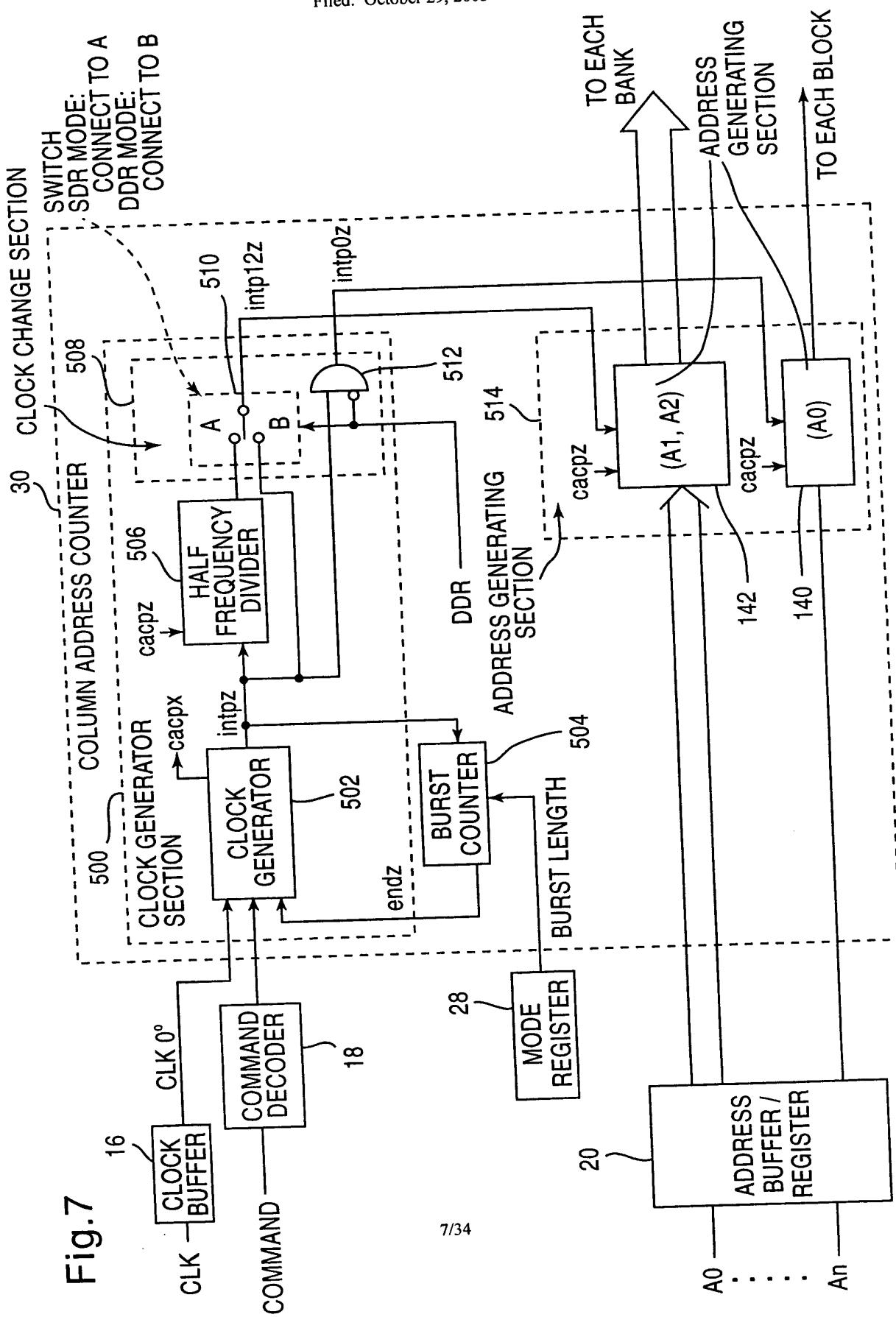


Fig. 6





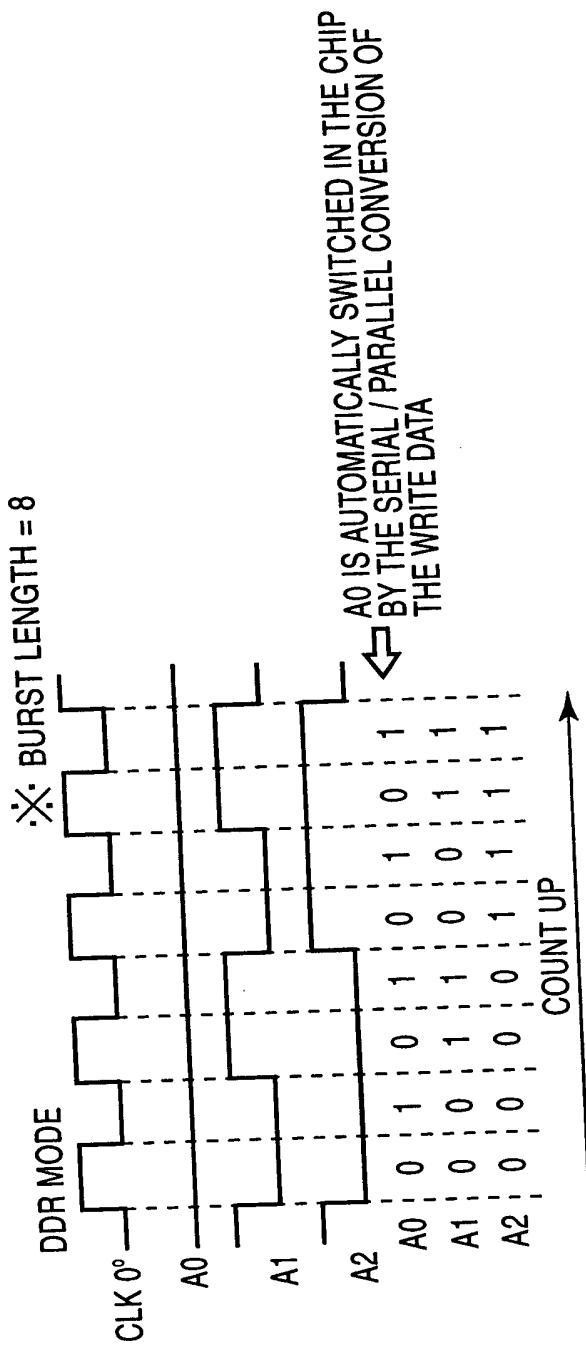


Fig.8(a)

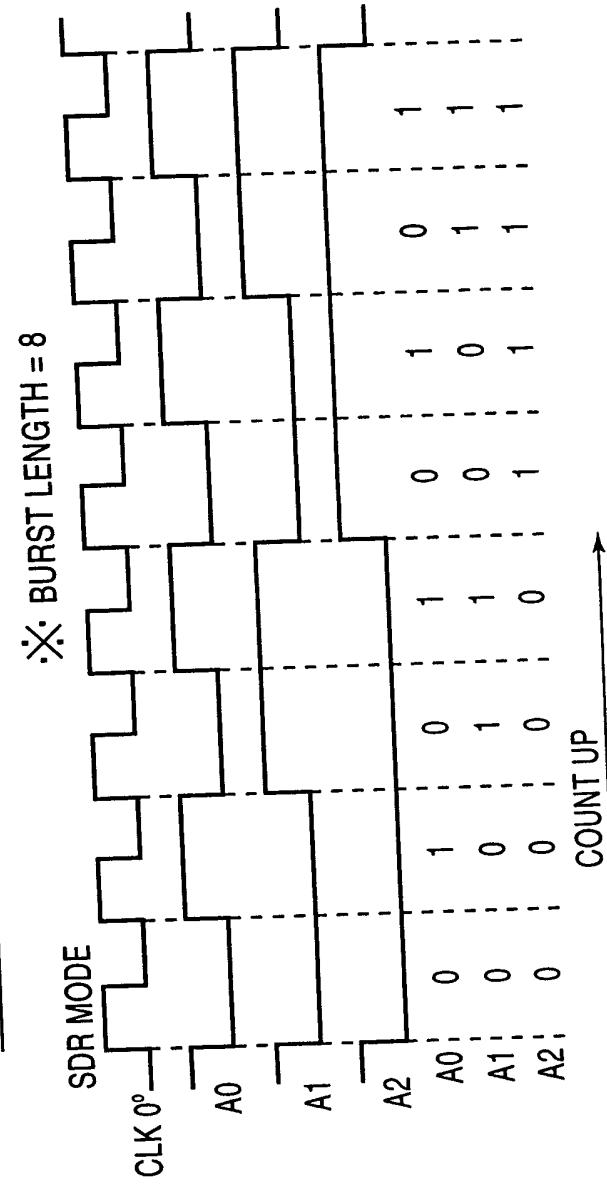
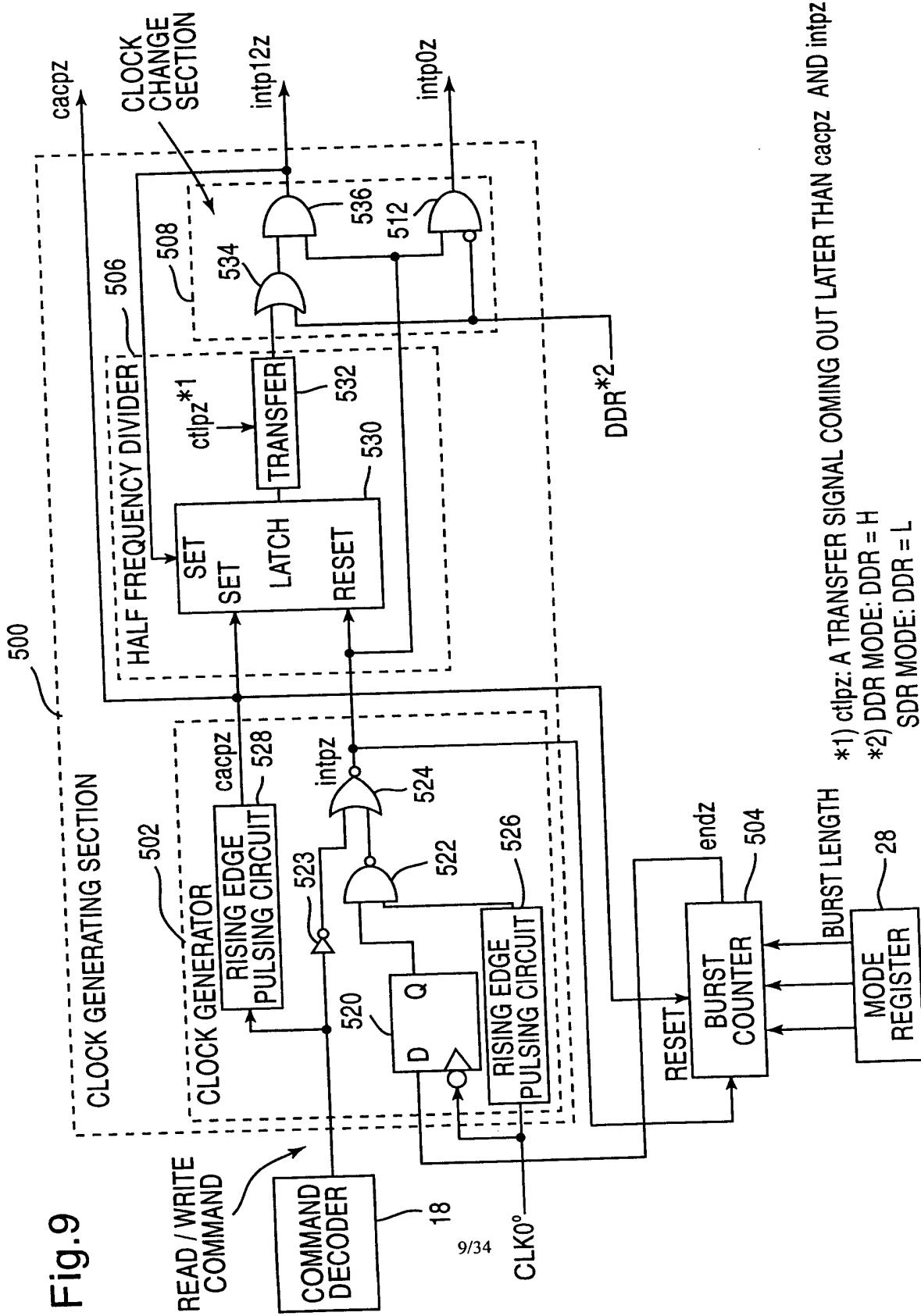


Fig.8(b)

Fig. 9



Title: Semiconductor Memory Device and Method of Controlling the Same
Inventor: Tatsuya KANDA, et al.
Divisional Application of U.S. Serial No. 09/264,672
Filed: October 29, 2003

Fig. 10

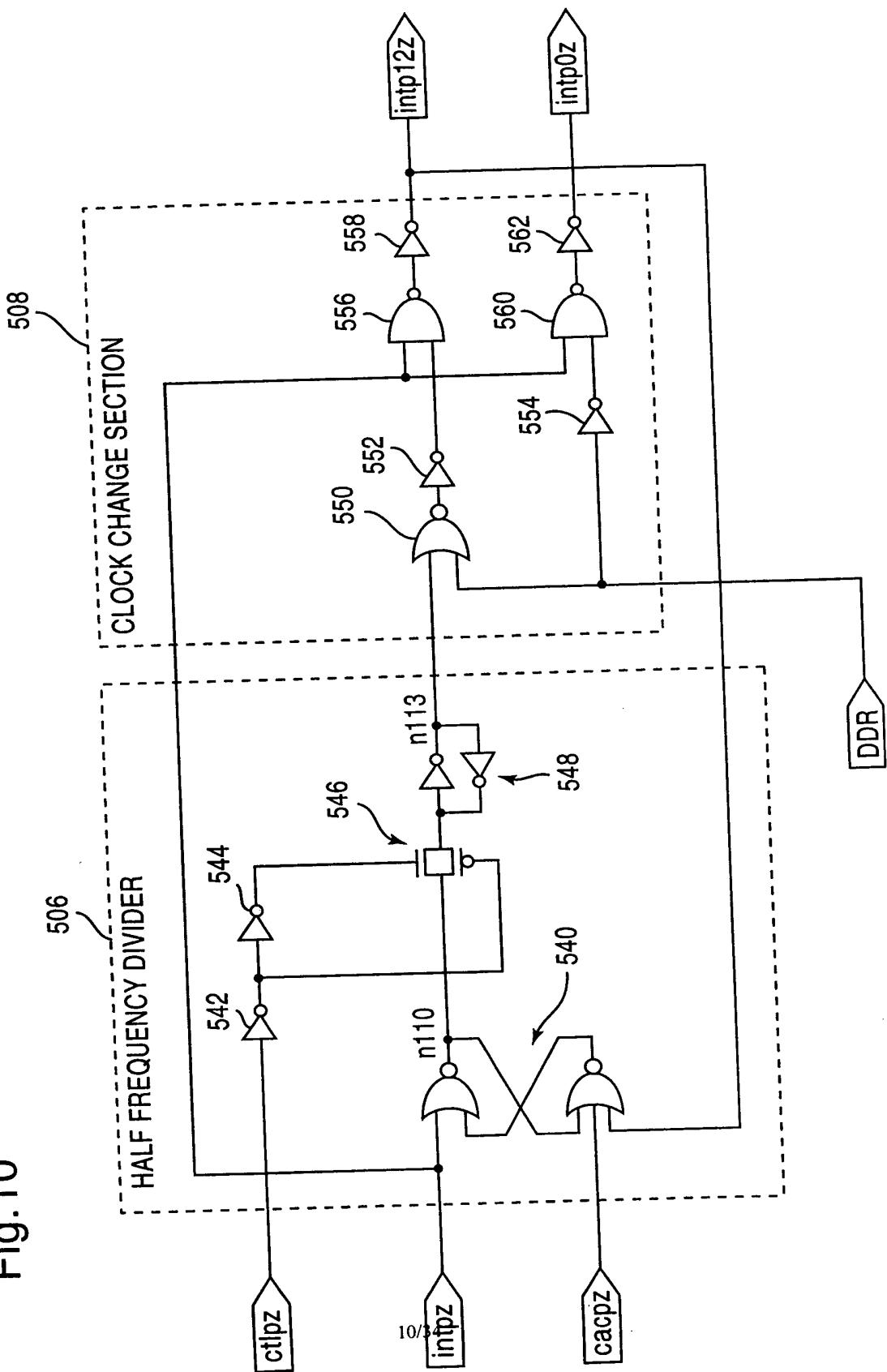


Fig. 11

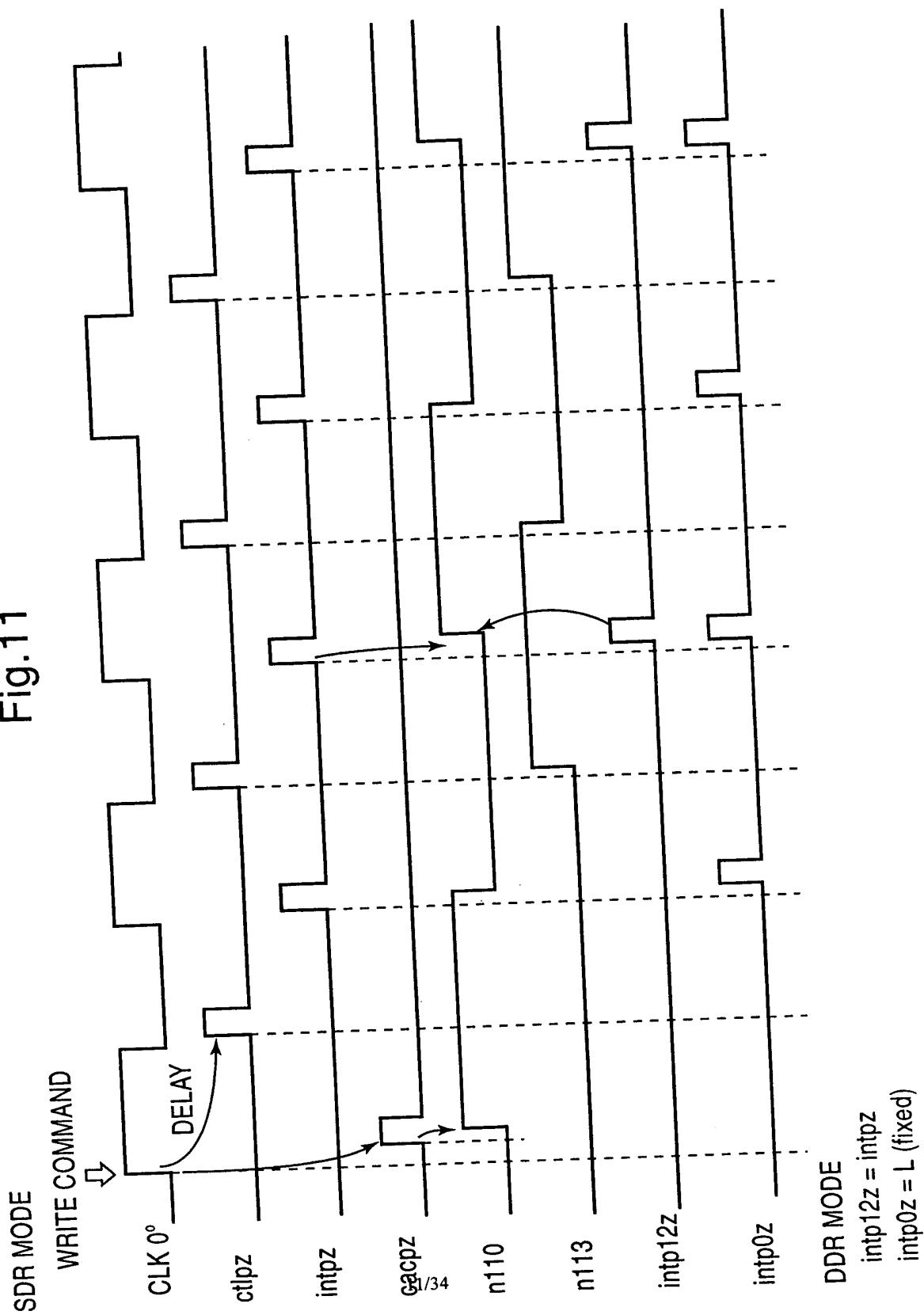


Fig. 12

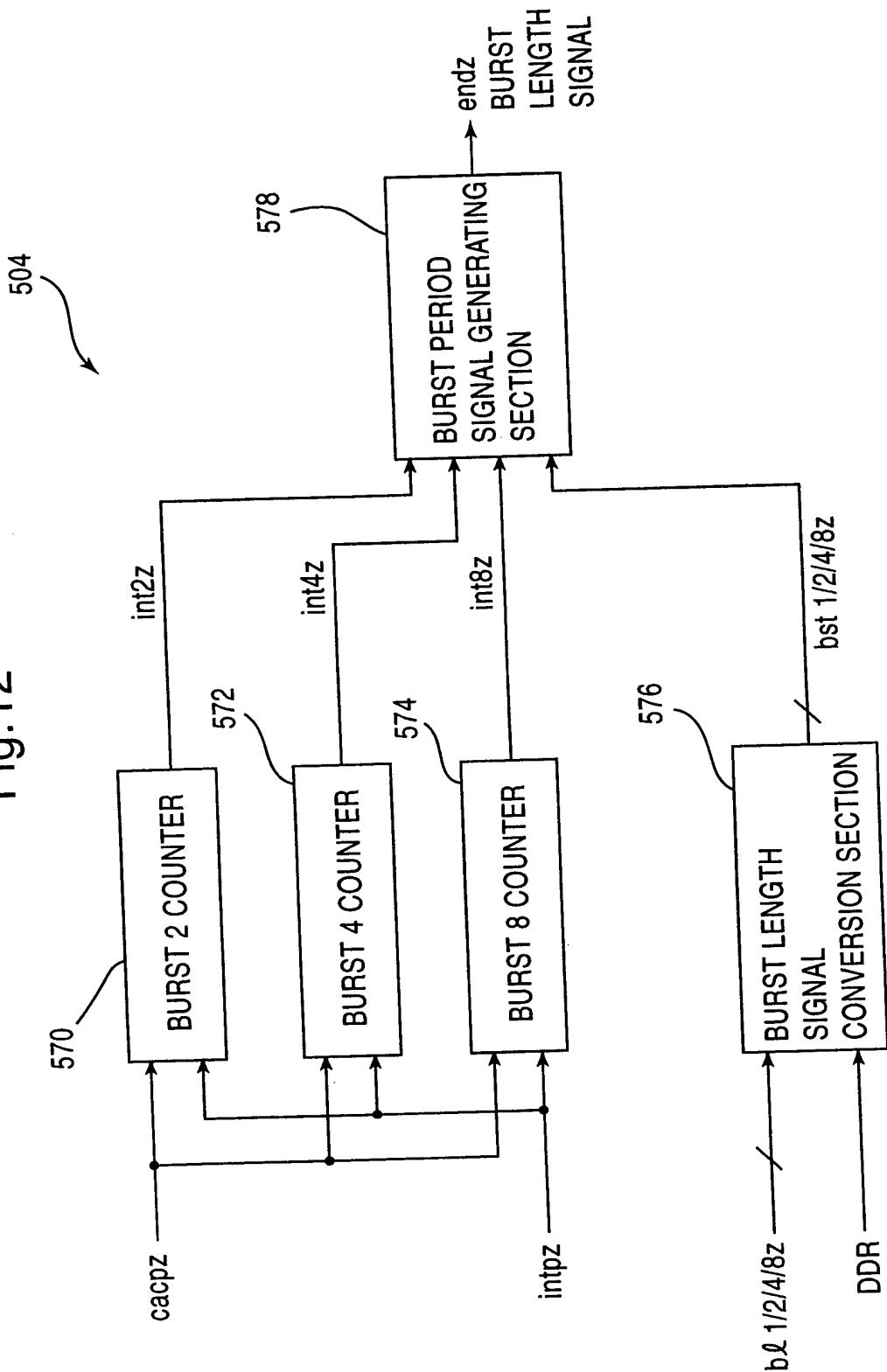


Fig. 13

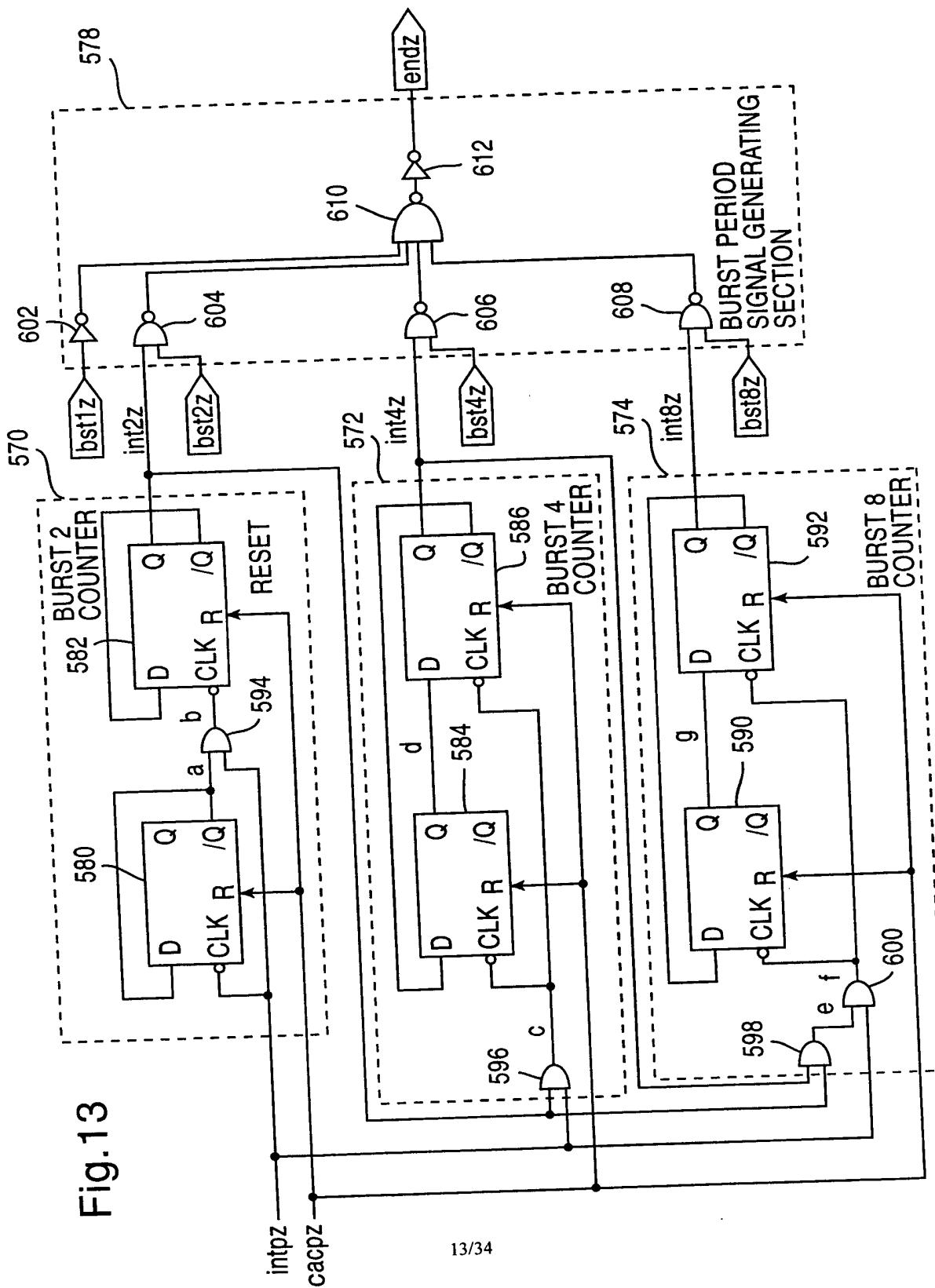


Fig. 14(a)

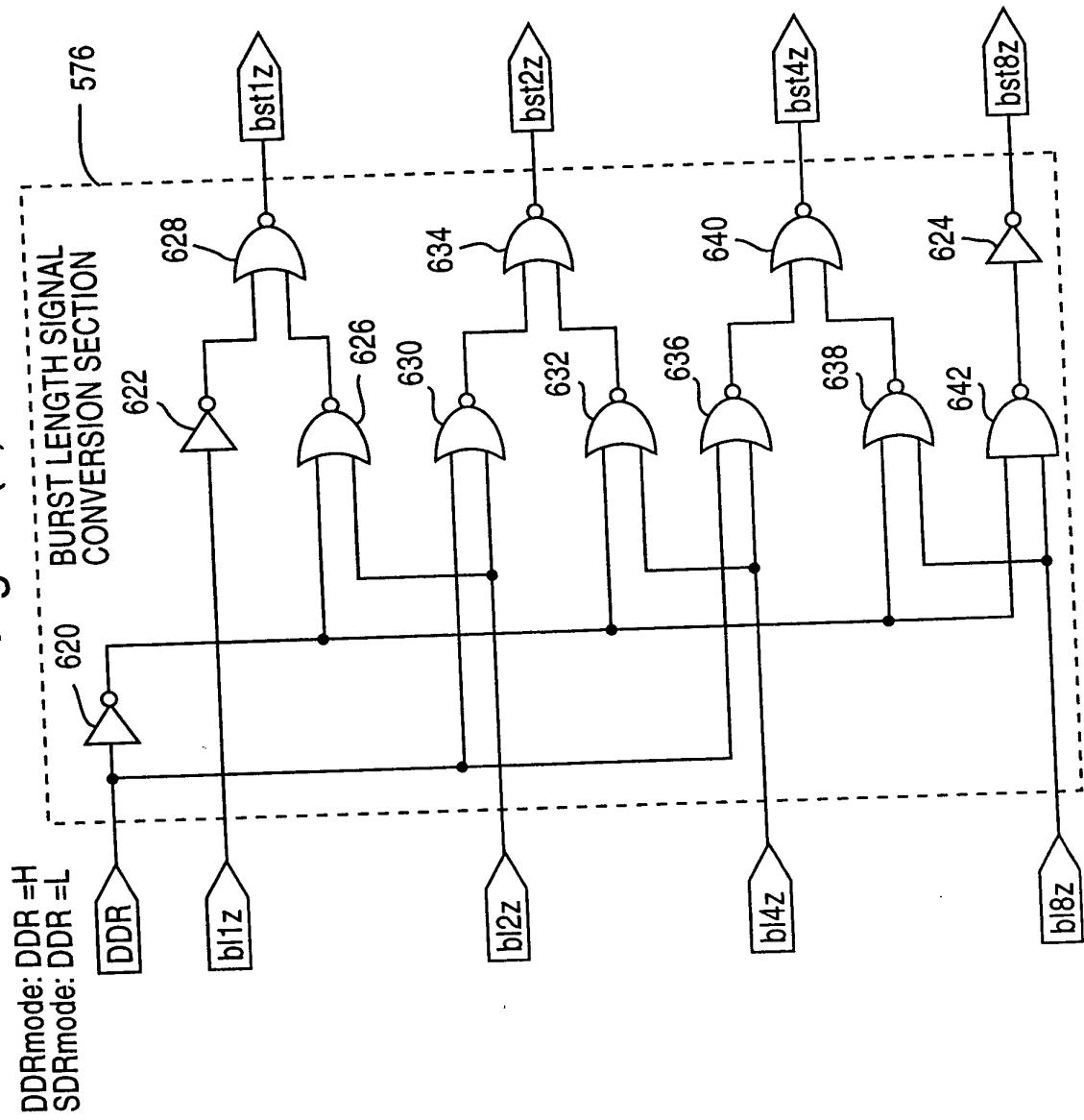
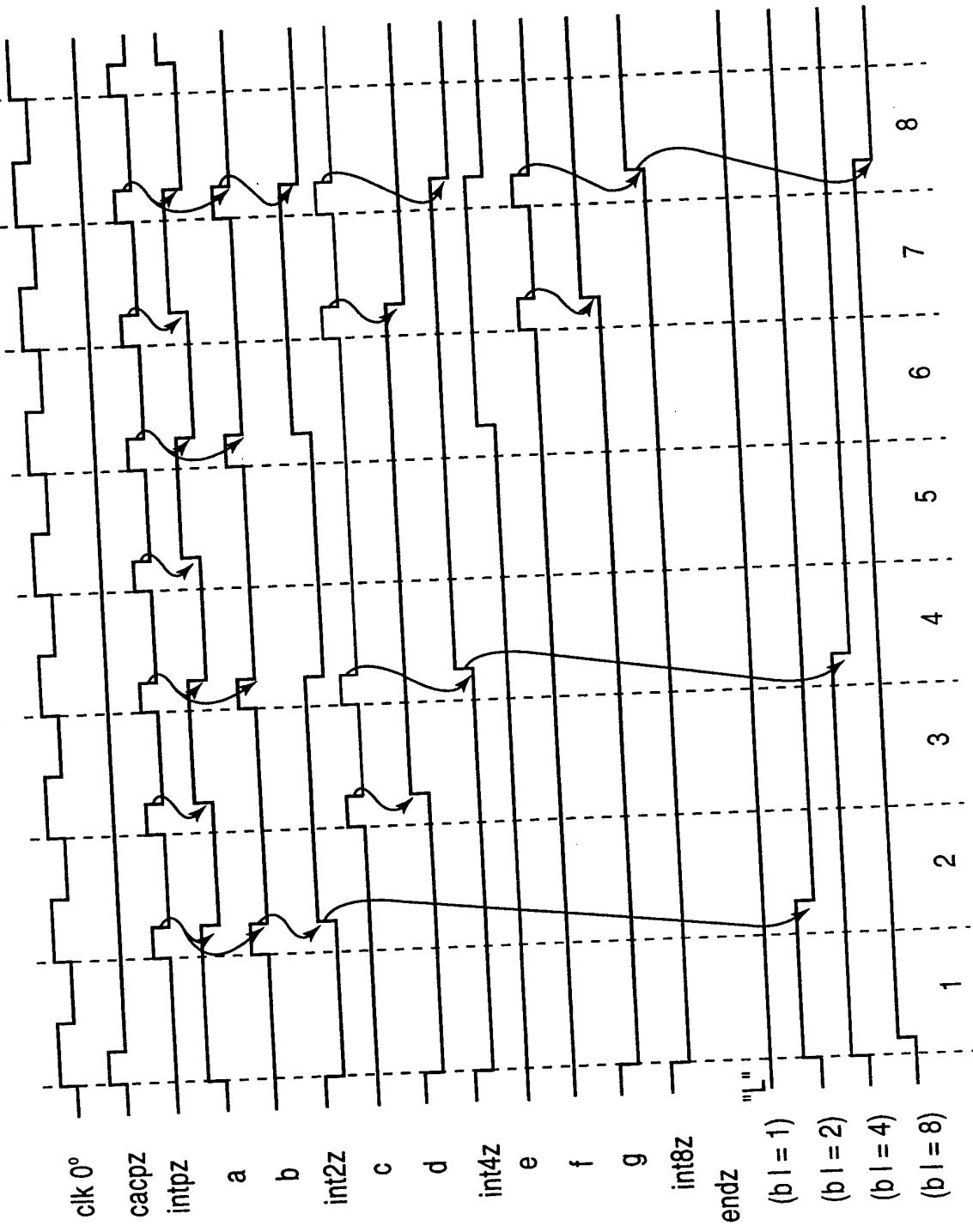
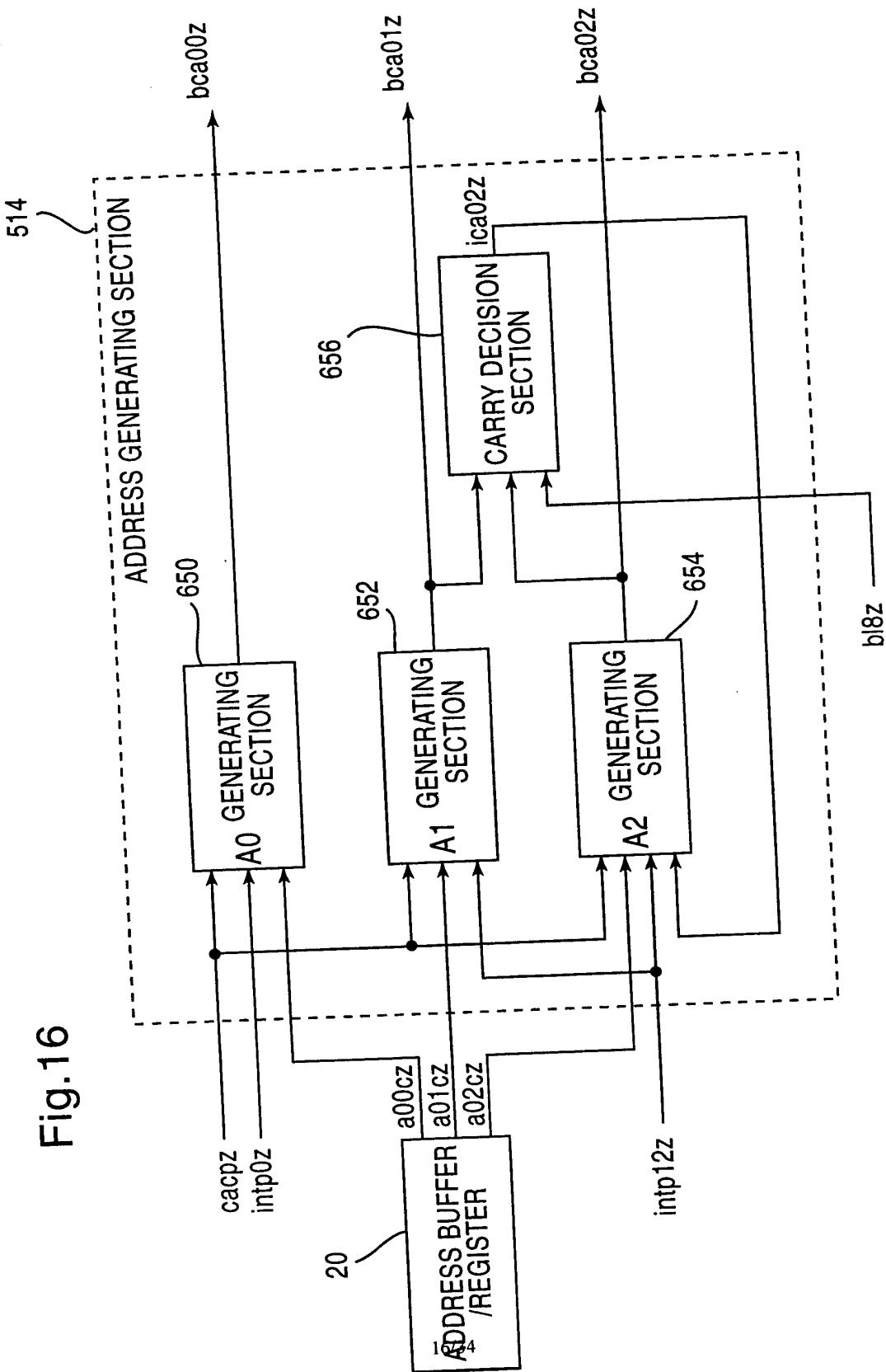


Fig. 14(b)

	DDR mode	SDR mode
bst1z	bl1z	bl1z
bst2z	bl2z	bl2z
bst4z	bl4z	bl4z
bst8z	bl8z	L

Fig. 15





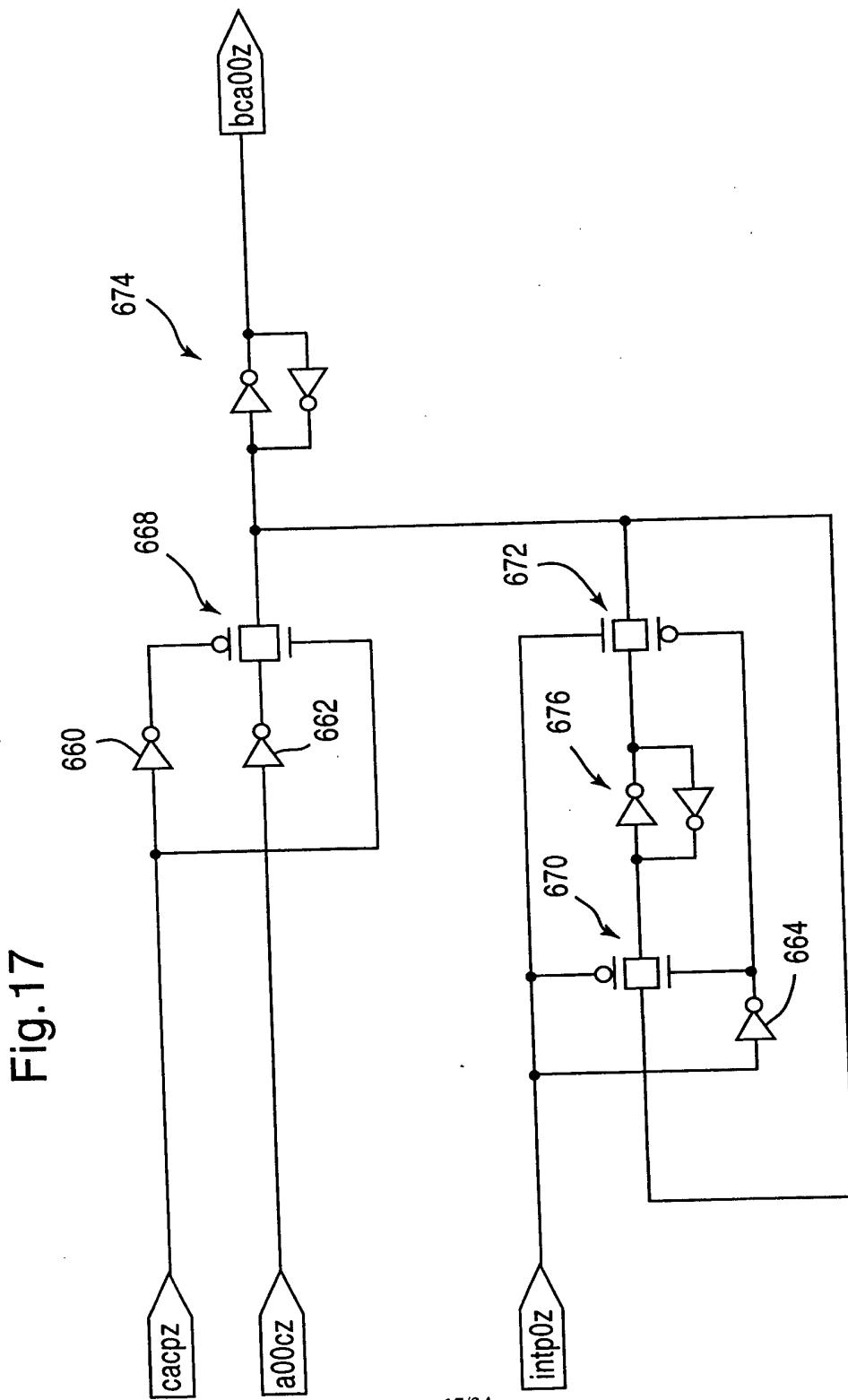


Fig. 18

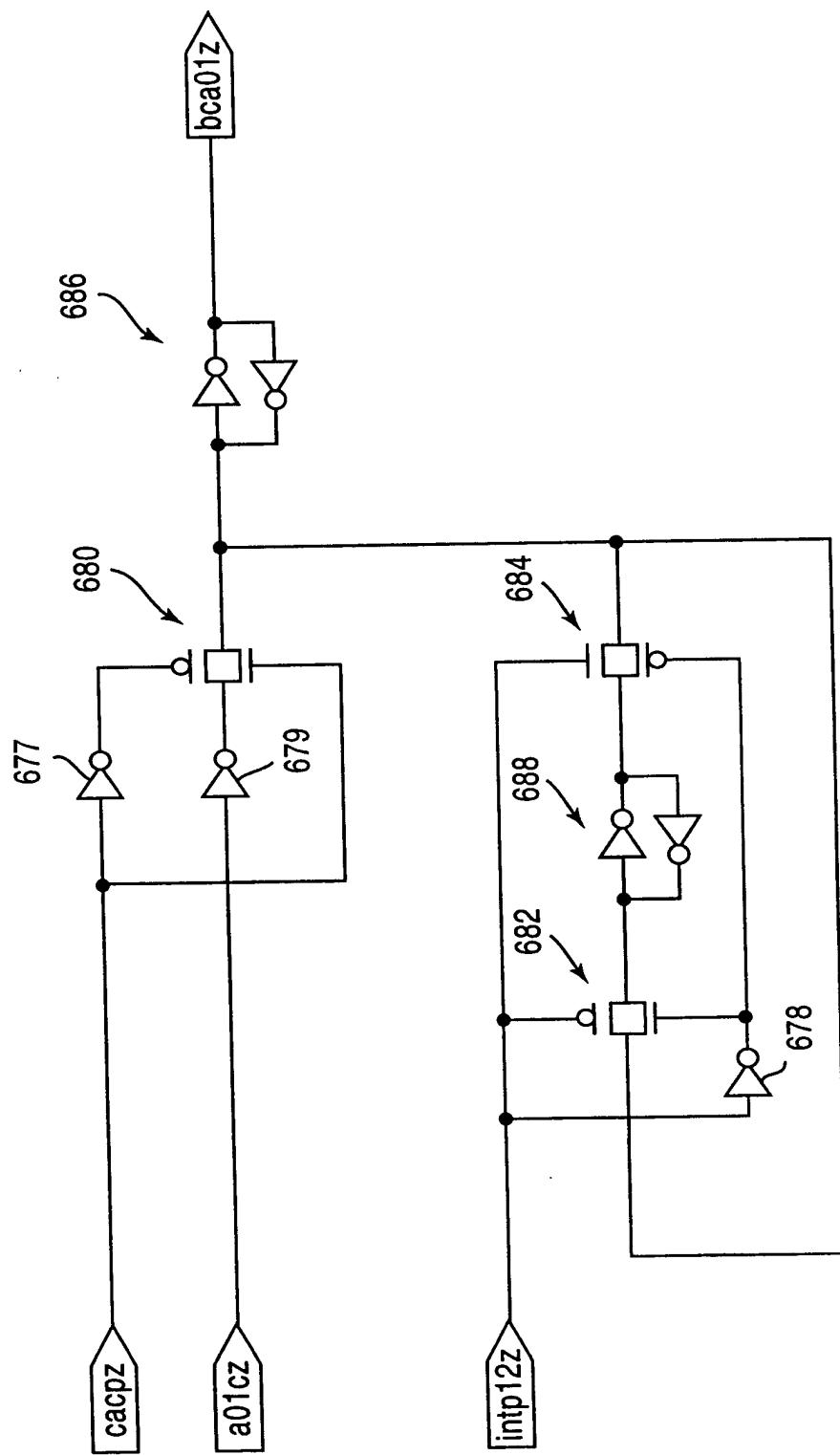


Fig.19

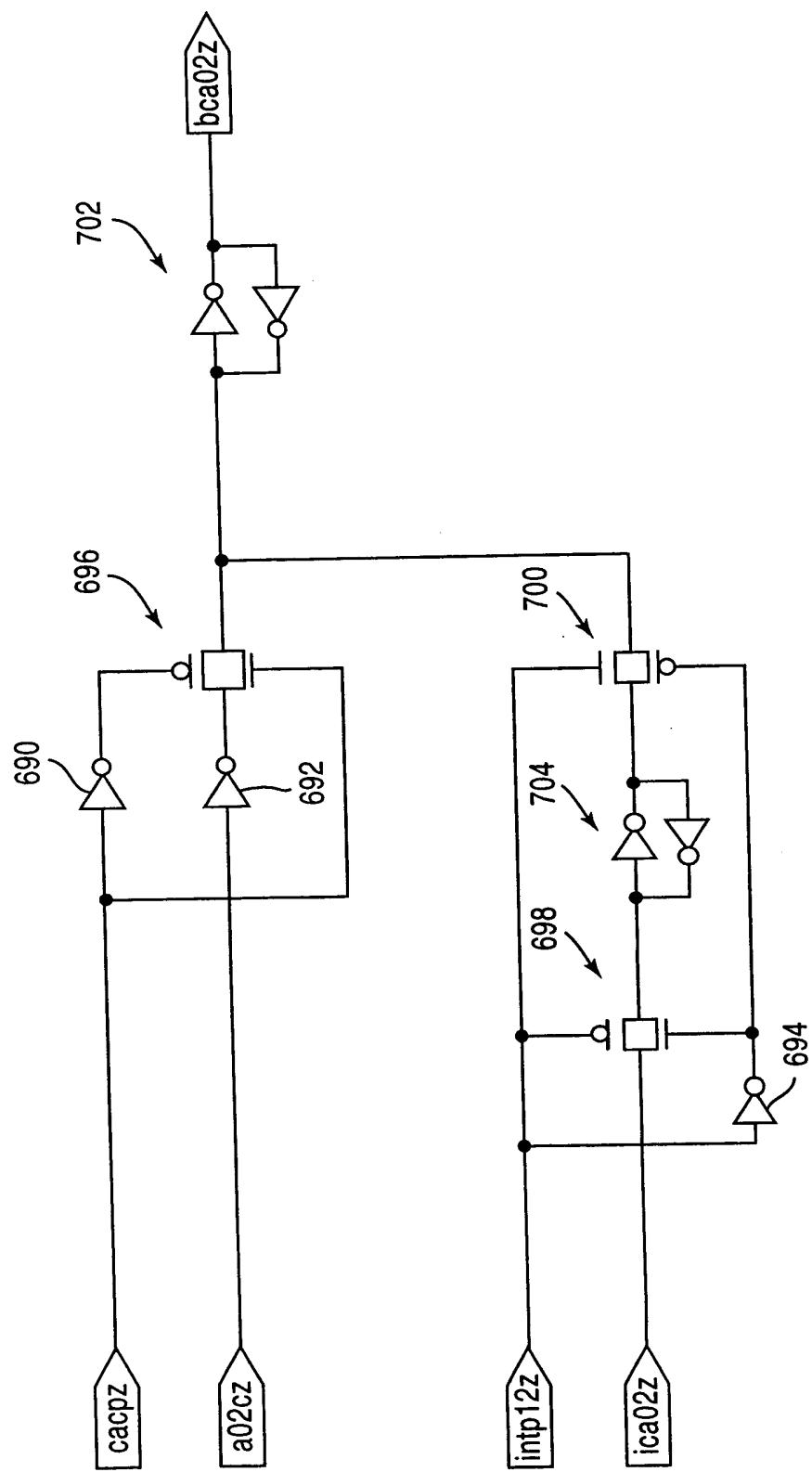
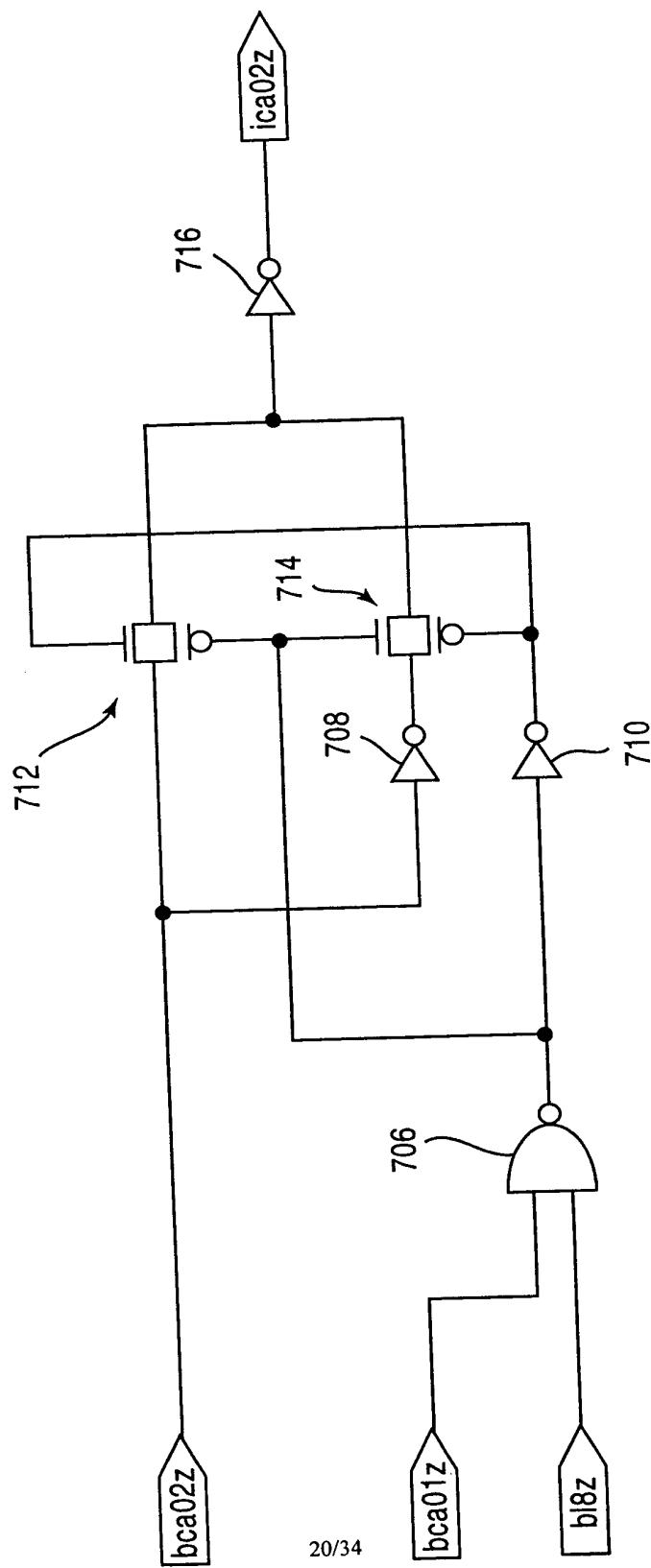
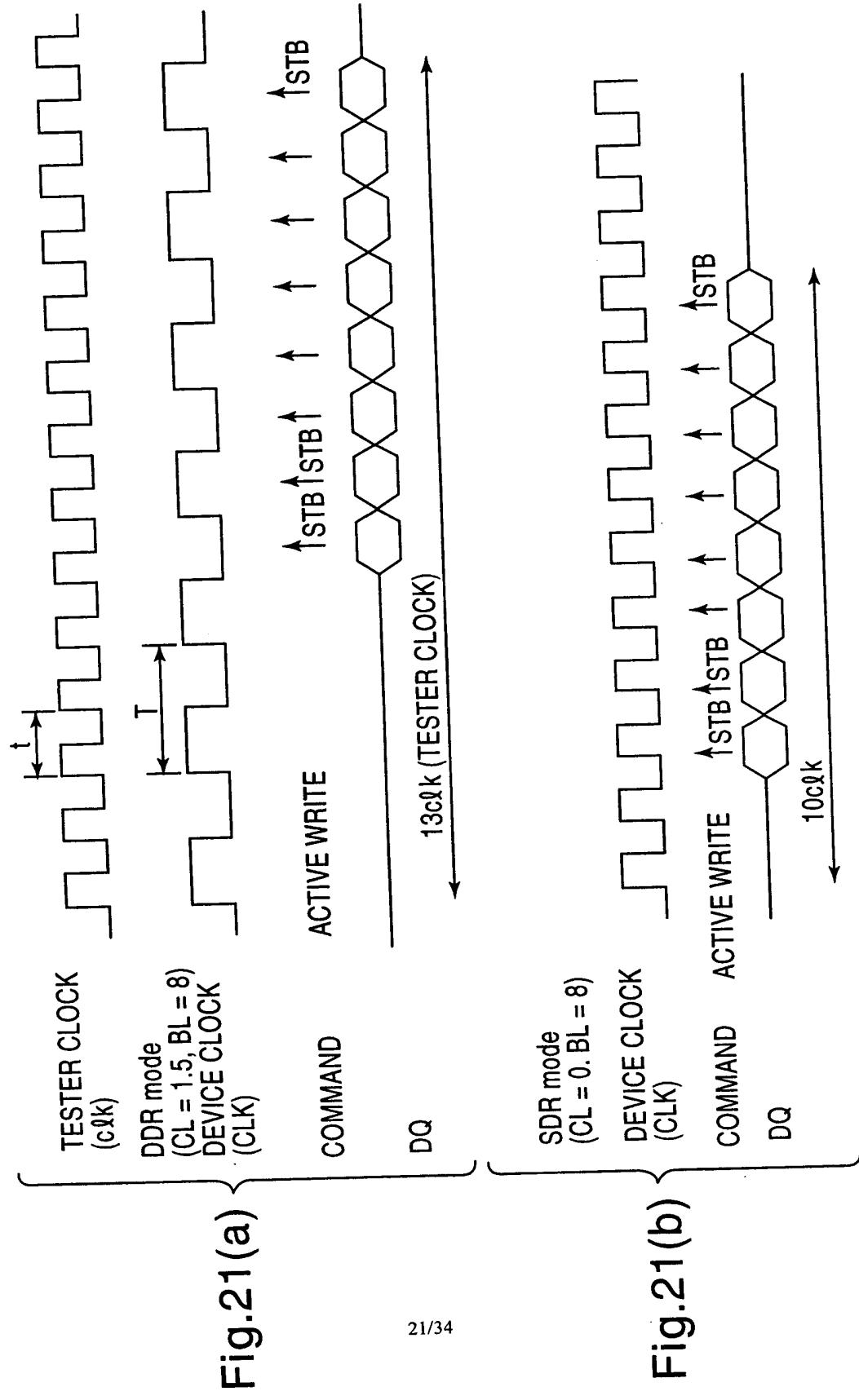
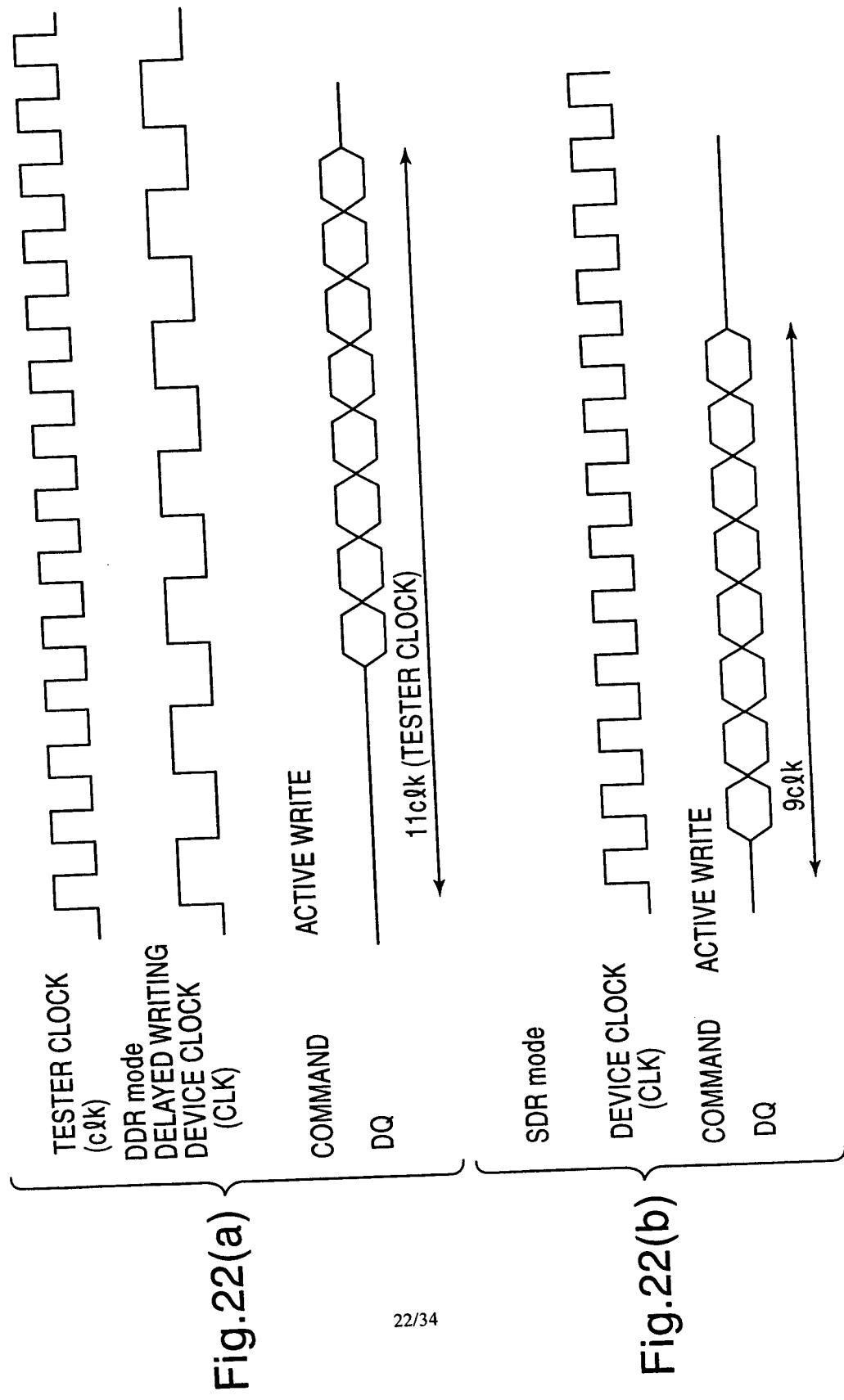


Fig.20







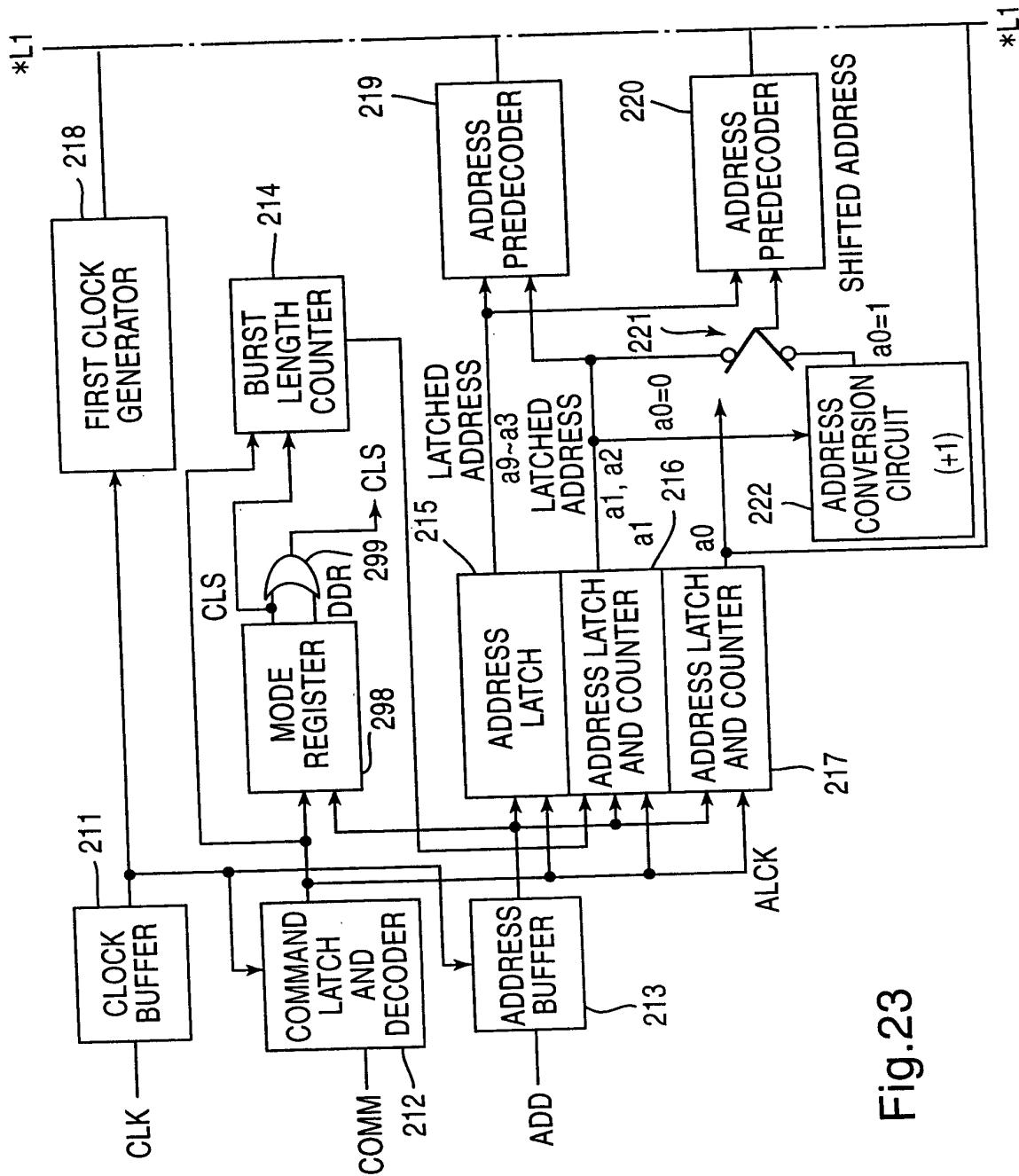


Fig.23

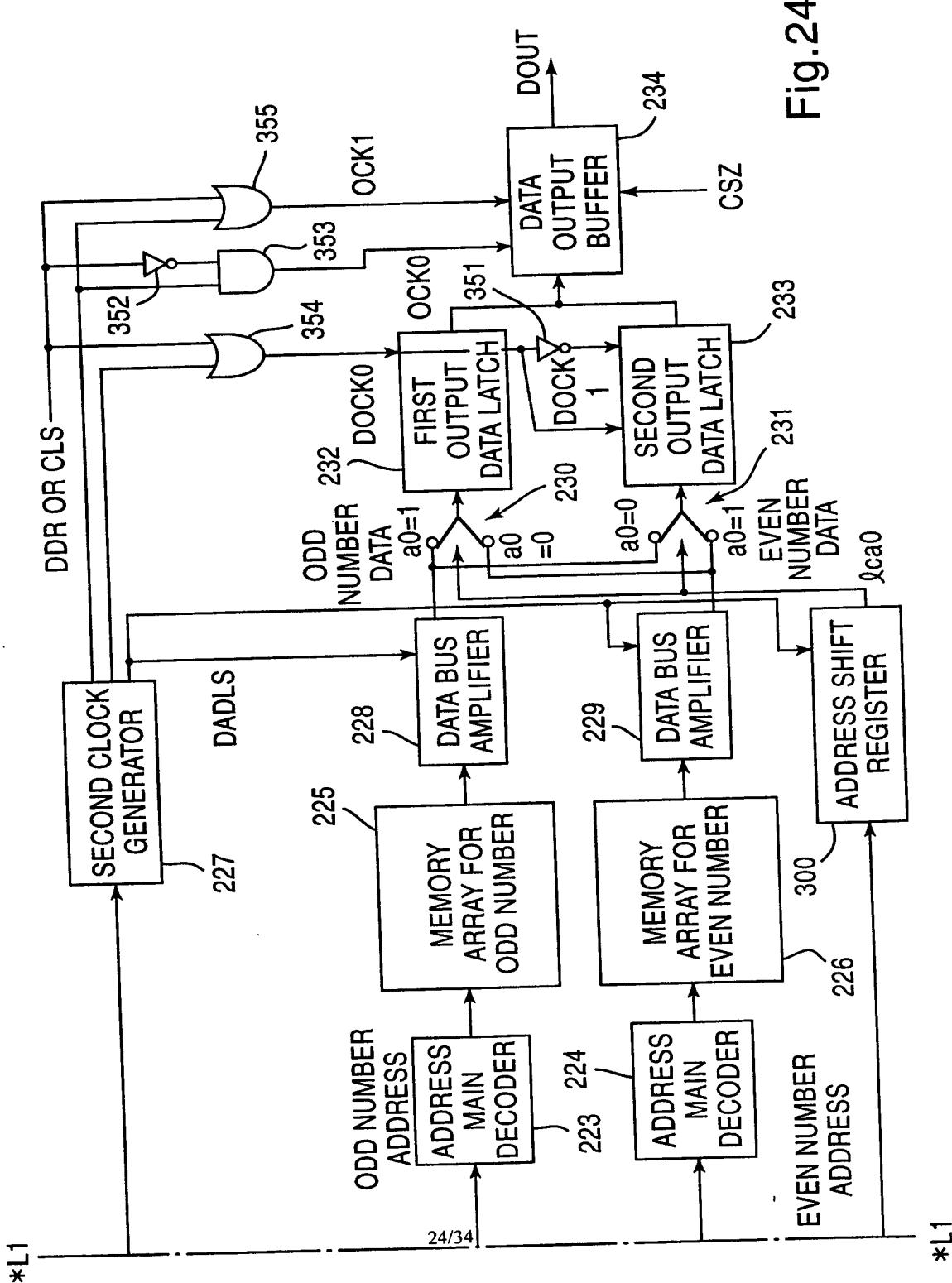


Fig.24

Fig.25

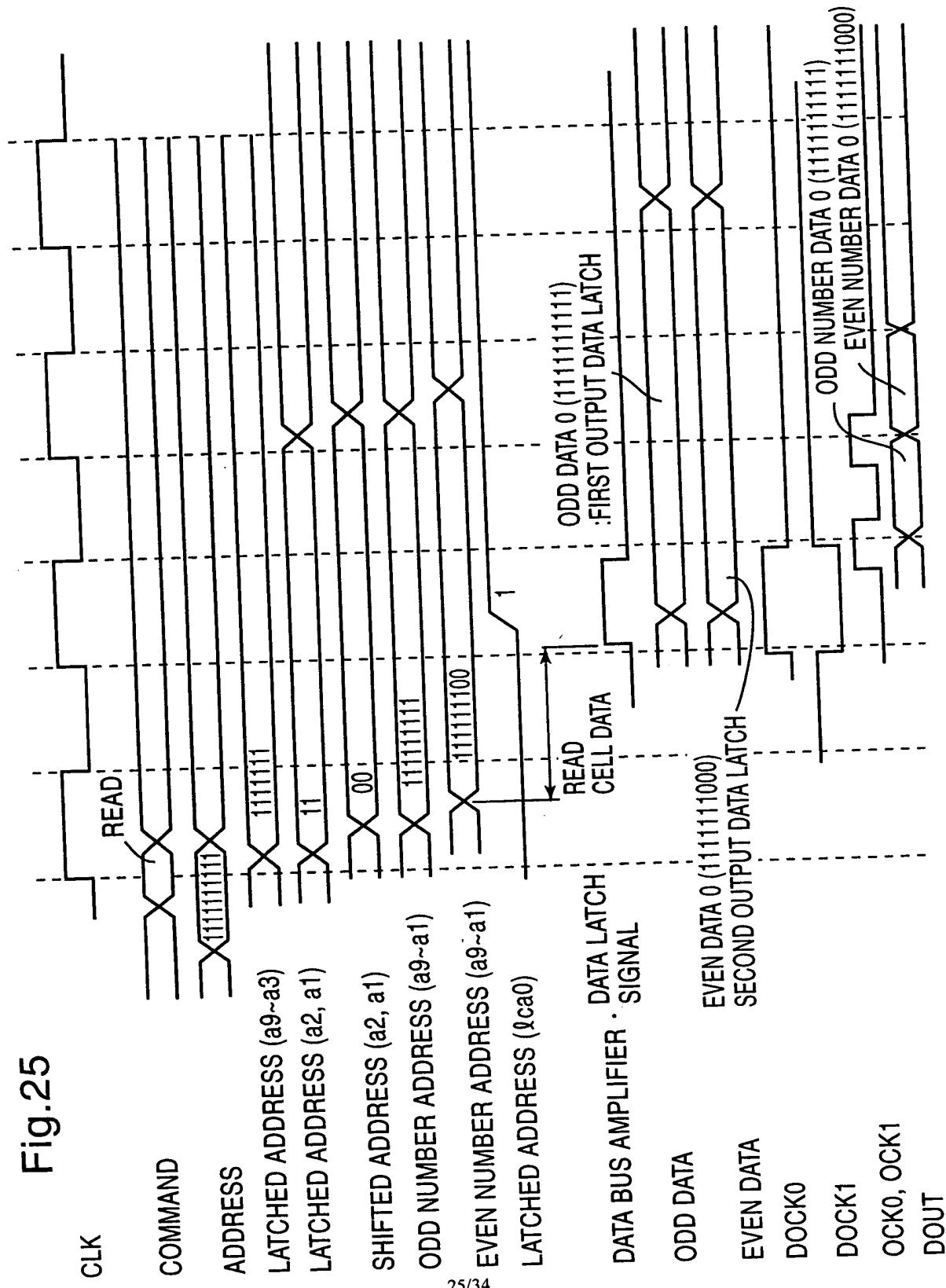


Fig. 26

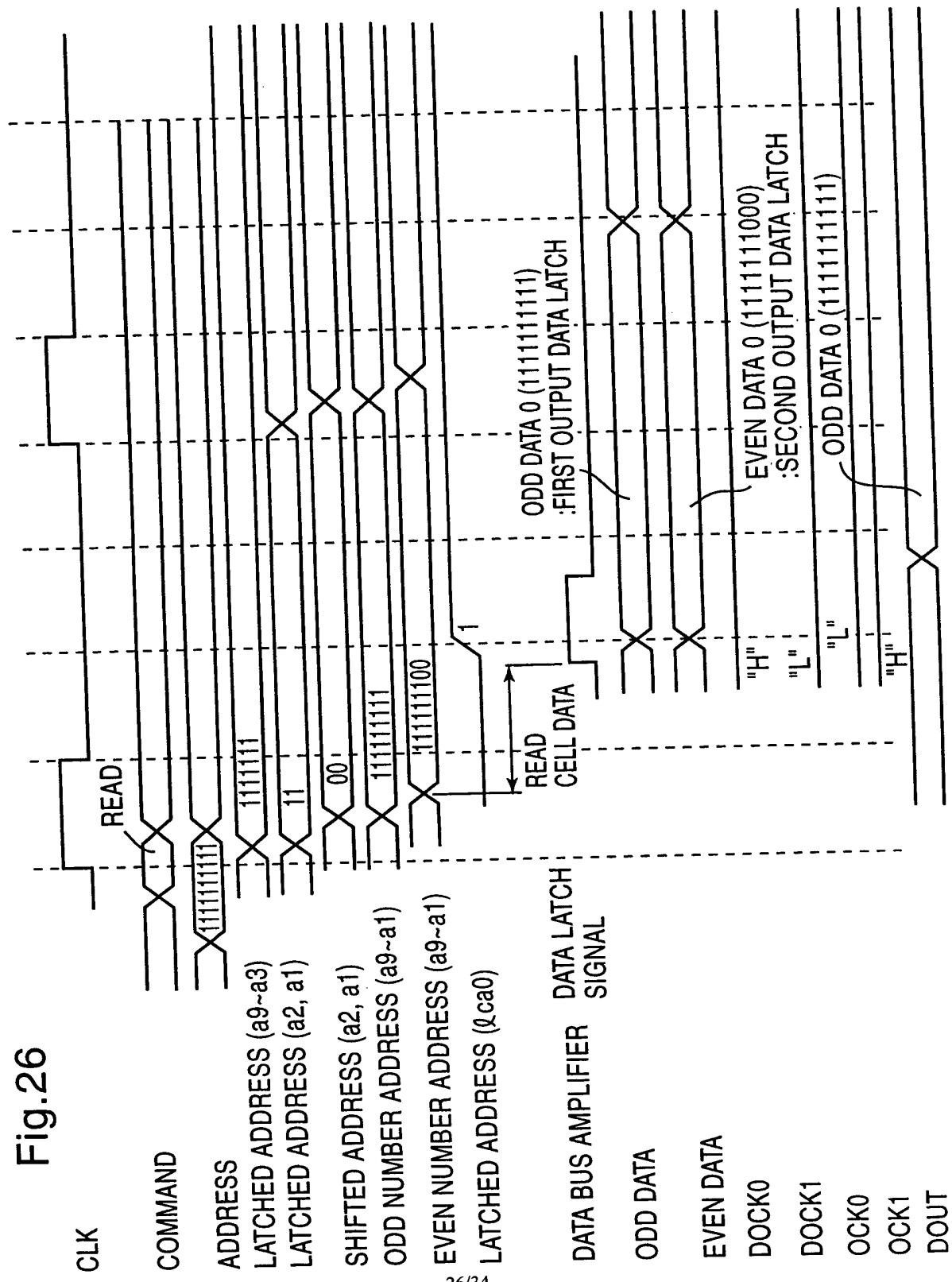
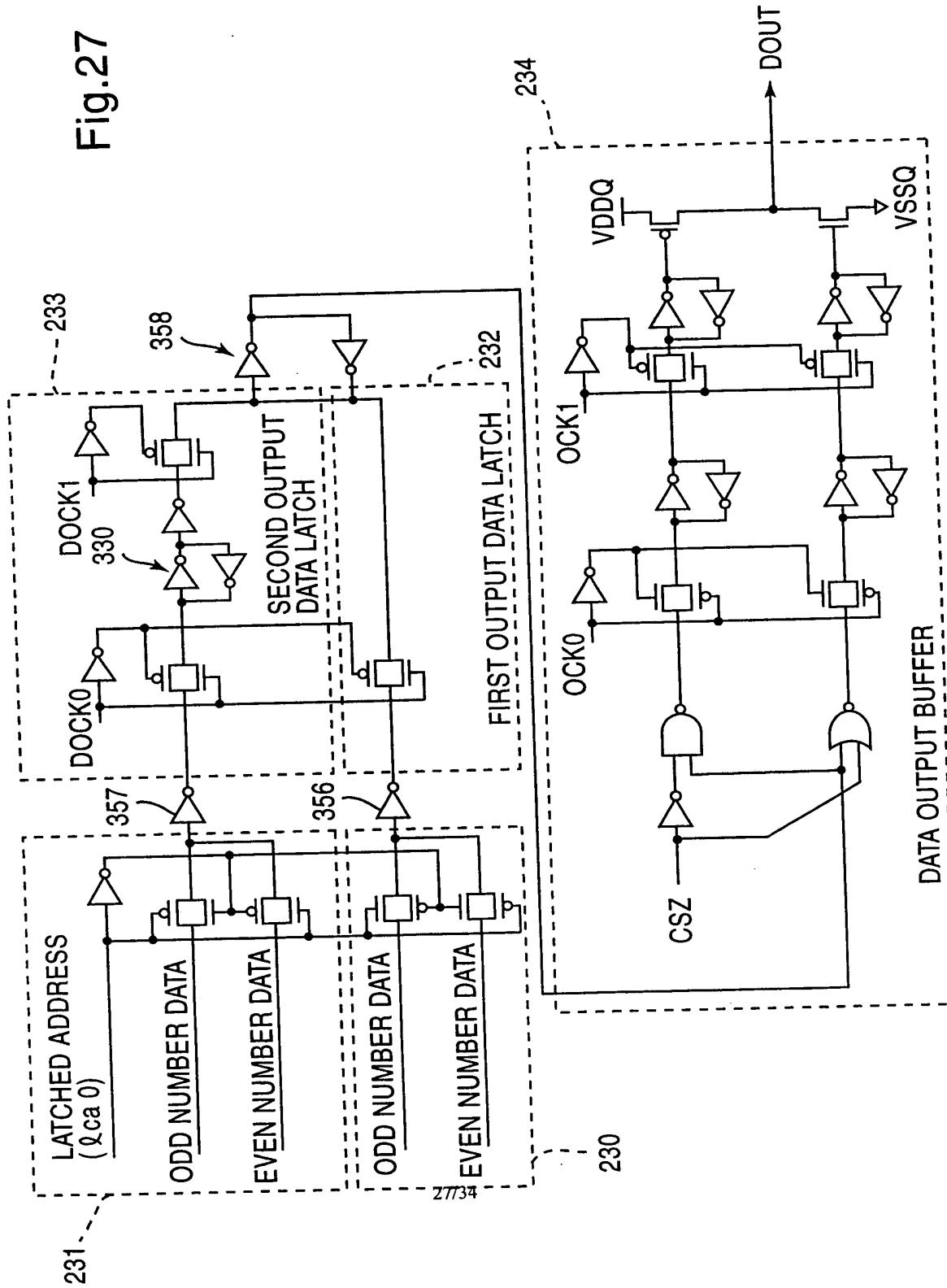


Fig. 27



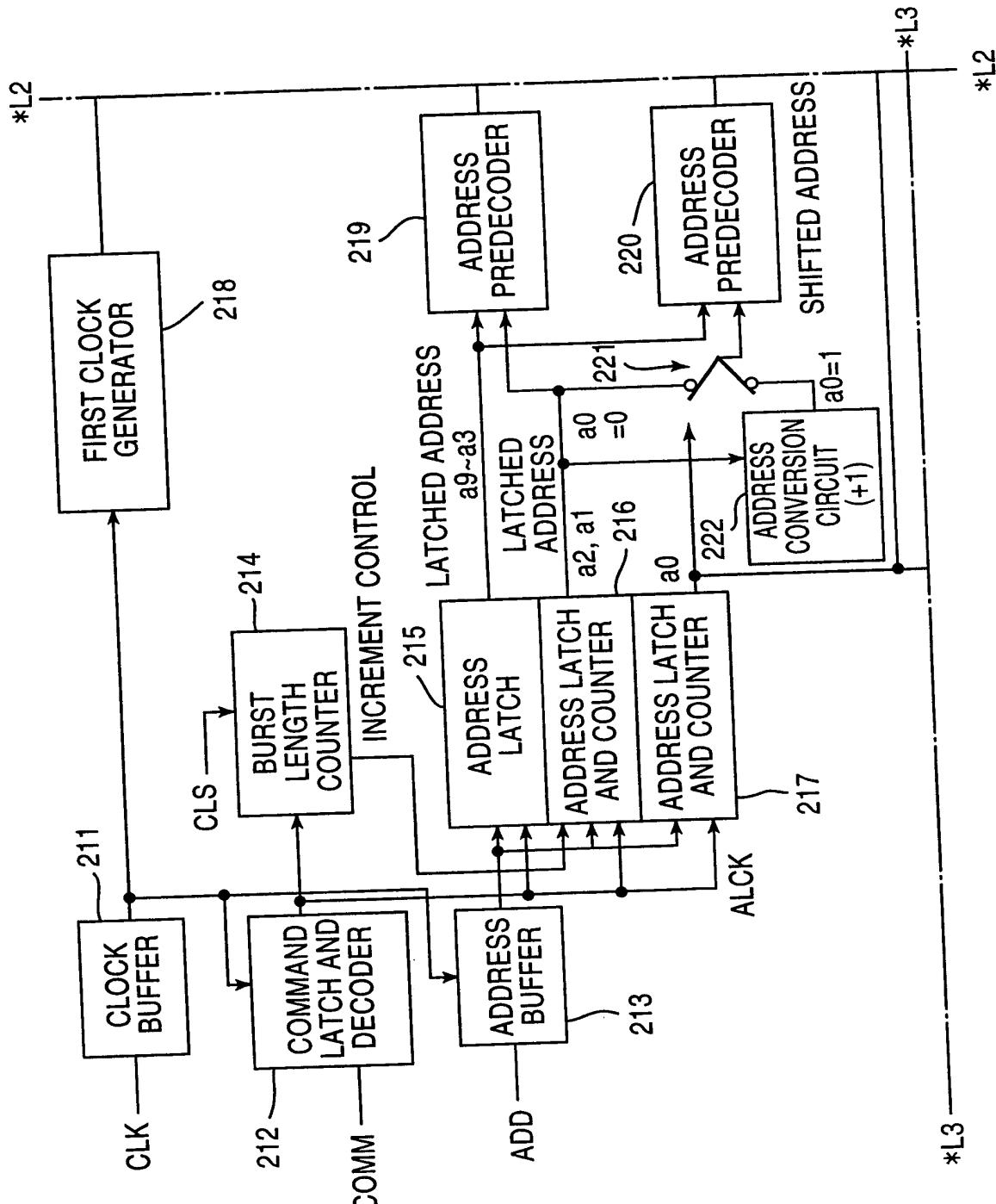


Fig.29

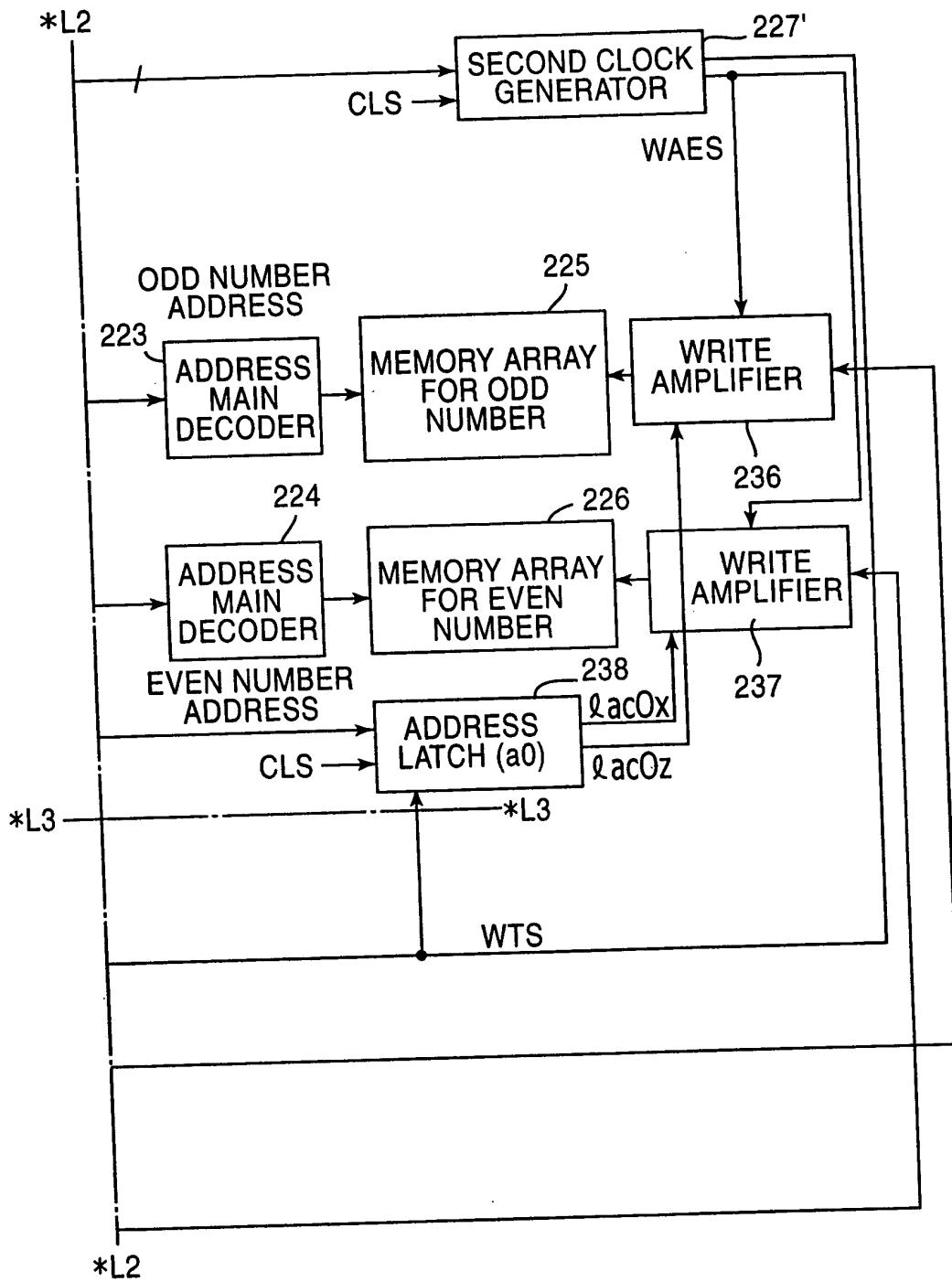


Fig.30

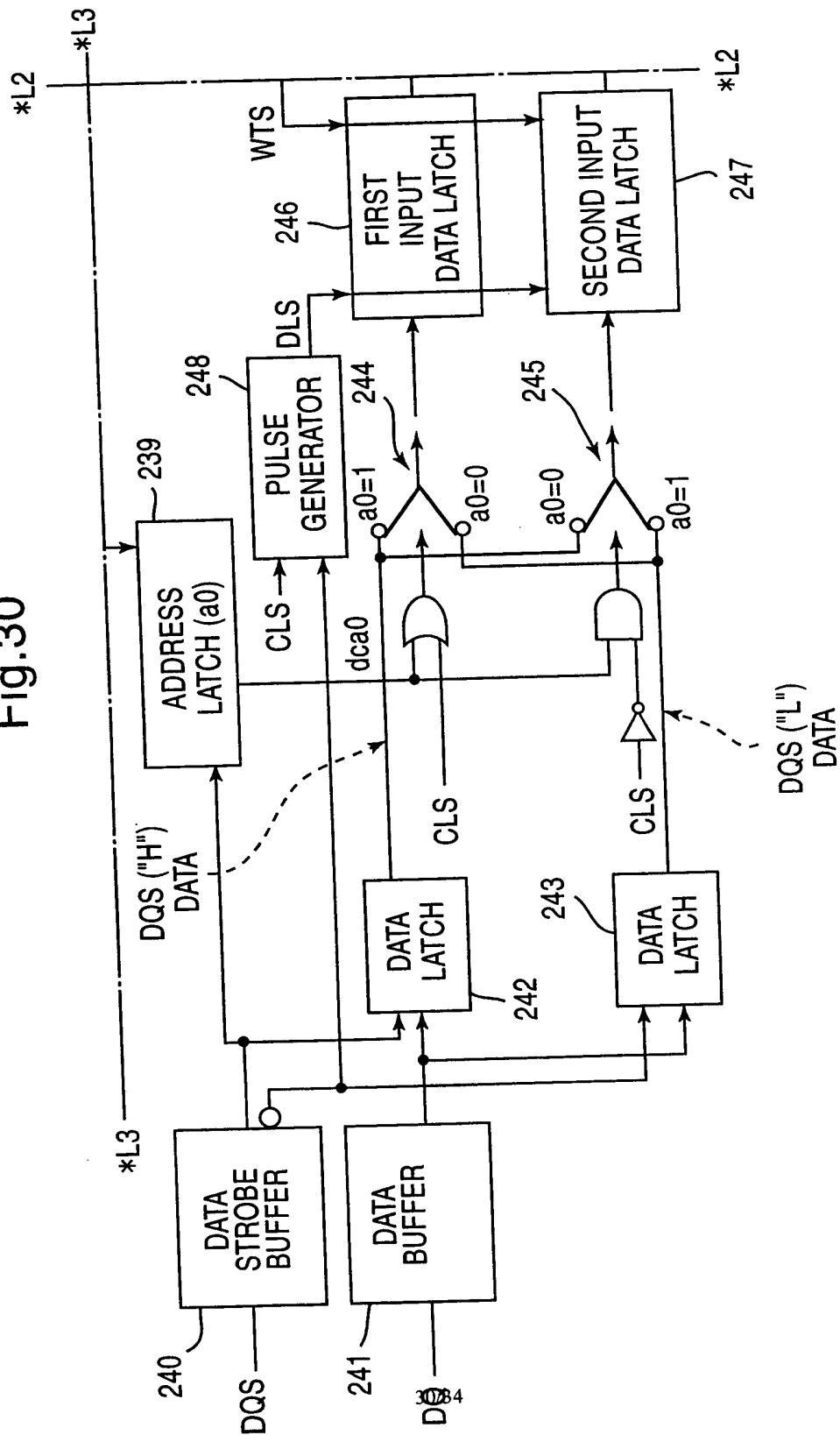


Fig.31

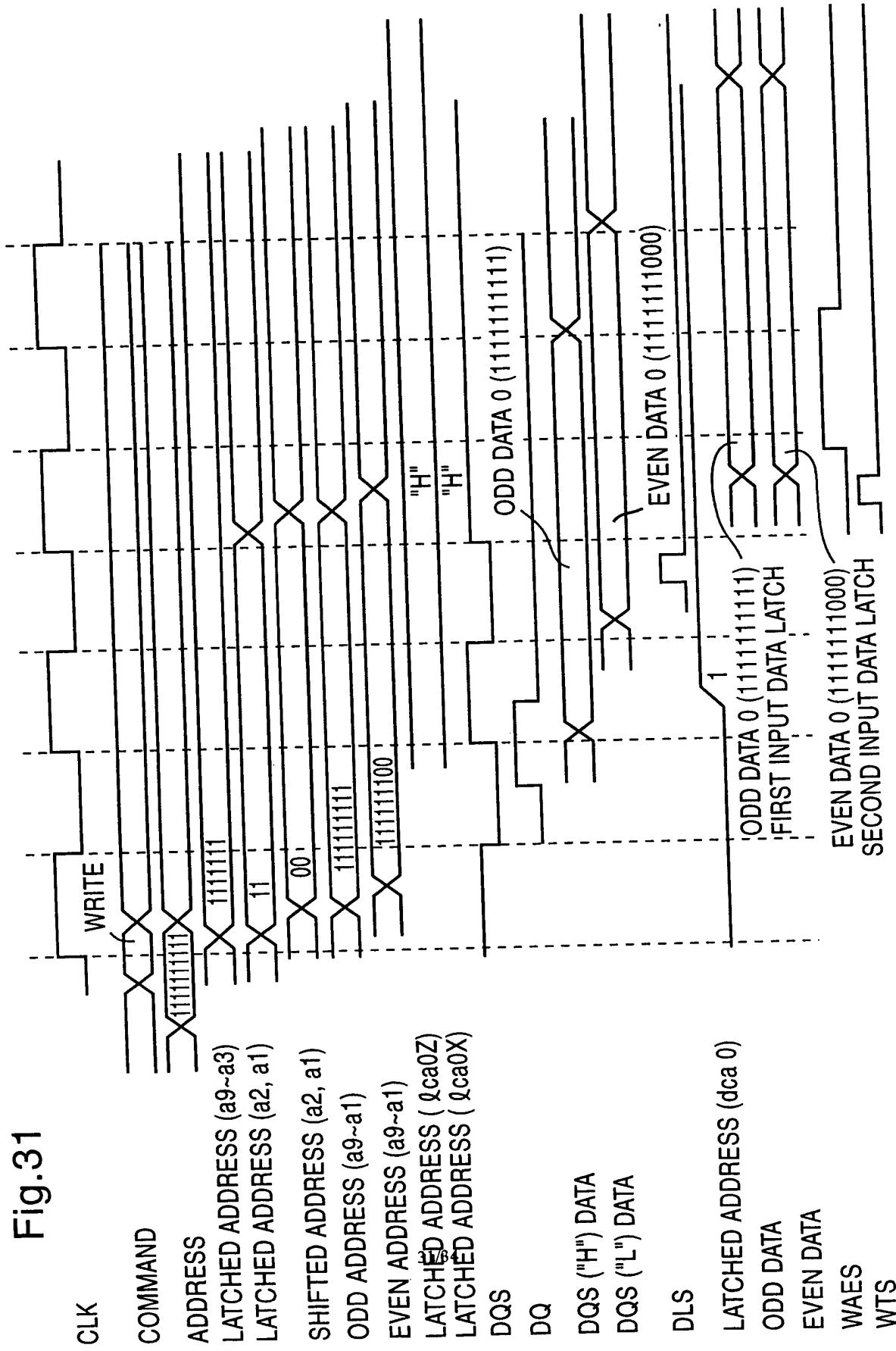


Fig.32

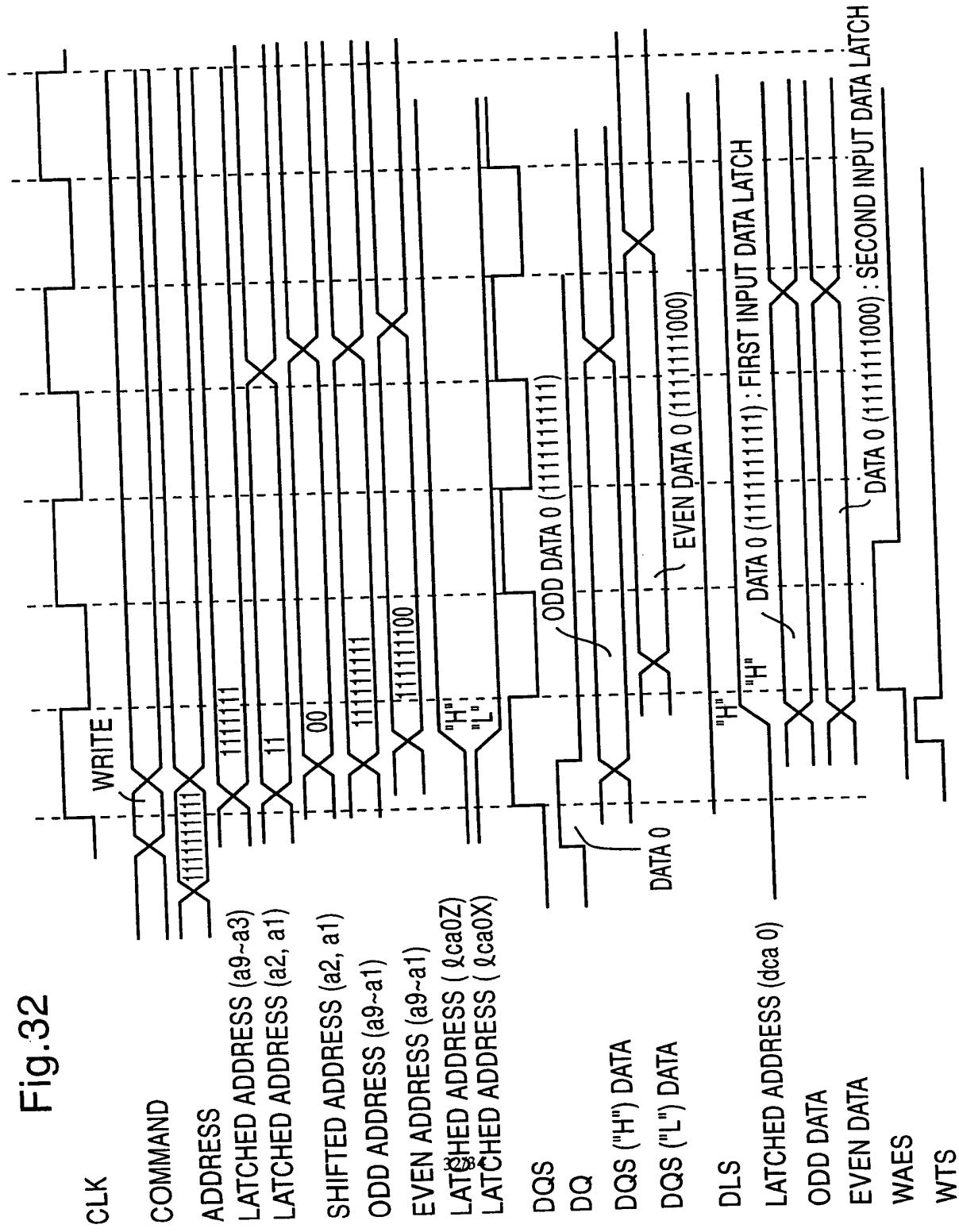


Fig.33

